A BCI SCALABLE SENSORY ACQUISITION SYSTEM FOR EEG EMBEDDED APPLICATIONS

by

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This dissertation was prepared under the direction of the candidate's thesis advisor, Dr. Bassem Alhalabi, Department of Computer and Electrical Engineering and Computer Science, and has been approved by the members of his supervisory committee. It was submitted to the faculty of the College of Engineering and Computer Science and was accepted in partial fulfillment for the requirements for the degree of Master of Science.

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Abstract

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Electroencephalogram (EEG) Recording has been through a lot of changes and modification since it was first introduced in 1929 due to rising technologies and signal processing advancements. The EEG Data acquisition stage is the first and most valuable component in any EEG recording System, it has the role of gathering and conditioning its input and outputting reliable data to be effectively analyzed and studied by digital signal processors using sophisticated and advanced algorithms which help in numerous medical and consumer applications. We have designed a low noise low power EEG data acquisition system that can be set to act as a standalone mobile EEG data processing unit providing data preprocessing functions; it can also be a very reliable high speed data acquisition interface to an EEG processing unit.

A BCI Scalable Sensory Acquisition System for

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Chapter 1

Introduction

1.0 Overview

Electroencephalograph (EEG) Data applications have gained significant attention in recent years which resulted in greatly increasing the research efforts in order to produce more valuable analysis techniques and introduce systems that would effectively utilize this data for various life usages. We have made it our responsibility to provide EEG data research personnel with an intelligent, low noise, low power and modular Brain Computer Interface (BCI) front-end EEG data acquisition system that will fit their needs and ease their efforts.

1.1 Problem Statement

BCI Design for EEG data acquisition has many limiting factors such as noise, power, cost and electrode placement constraints [2] [3]. Also most of the available BCI implementation do not support multiple interfaces or mobile operation capability and lack intelligent intermediate stages that would support high speed data transfer for real time operation and manage the data acquisition process. Also, after surveying the current solutions we couldn't find a BCI design that acts as a customizable interface that could be utilized in various applications according to researcher's needs. It is our intention to introduce a solution that would address these described constraints and could be used as a development platform for EEG embedded applications.

1.2 EEG Overview

Electroencephalography (EEG) is the recording of electrical activity along the scalp produced by the firing of neurons within the brain [33]. It is also defined as the record of the oscillations of brain electric potentials recorded from electrodes (1-256 electrodes) attached to the human scalp [47] as indicated in Figure 1. In electrical terms EEG represents the difference in voltage between two different cerebral locations plotted over time [9].

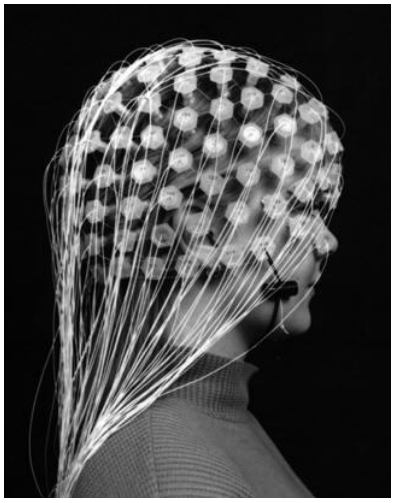


Figure 1.1. **A geodesic net with 128 electrodes from [47].**

1.2.1 EEG history. Since first introduced by Hans Berger in 1929, EEG measurements basics have not changed much [2], but the technological advancements and techniques have contributed to making EEG signals measurements and acquisition more effective and sophisticated. In 1924, Berger made the first EEG recording in man history and called it Electroencephalogram. Using the EEG he was also the first to describe the different waves or rhythms which were present in the normal and abnormal brain, such as the alpha wave rhythm (8–12 Hz), also known as Berger's wave and its

suppression (substitution by the faster beta waves) when the subject opens the eyes. He also studied and described for the first time the nature of EEG alterations in brain diseases such as epilepsy [33].

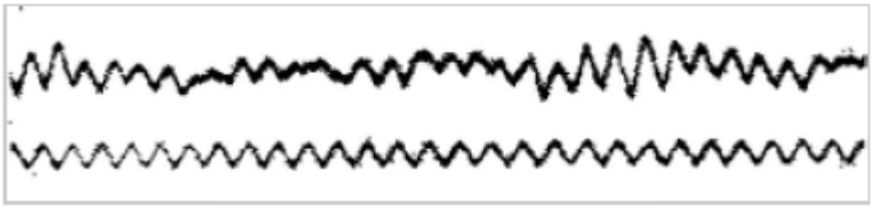


Figure 1.2. **An early EEG recording done by Berger from [33].**

Berger experimented using different methods and techniques in order to capture the EEG signal activity. His method involved inserting silver wires under the patient's scalp, one at the front of the head and one at the back. Later he used silver foil electrodes attached to the head by a rubber bandage. Using a double-coil Siemens recording galvanometer allowed him to record electrical voltages as small as one ten thousandth of a volt [33]. The resulting output, up to three seconds in duration, was then photographed as shown in Figure 1.2.

1.2.2 EEG signal analysis. EEG signals are composed of different oscillations named "rhythms" [5] [14]. These rhythms have distinct properties in terms of spatial and spectral localization. These EEG signals' amplitudes are approximately less than 100μV and less than 100Hz in frequency [2]. Table 1.1 lists some of the EEG signals, its frequency ranges and it associated activities.

Table 1.1

EEG Signals' frequency ranges and associated activities from [23].

Name	**Frequency (Hz)**	**Association**
Delta	1 - 4	Sleep, repair, complex problem solving.
Theta	4 – 8	Creativity, insight, deep states.
Alpha	8 – 12	Alertness, peacefulness, readiness, meditation.
Beta	13 – 21	Thinking, focusing, sustained attention.
SMR	12 – 15	Mental alertness, physical relaxation
High Beta	20 – 32	Intensity, hyper-alertness, anxiety.
Gamma	30-70 [50]	Cognitive processing, learning.

1.2.3 EEG applications. EEG signals could be utilized in various applications, but clinical applications are the most demanding amongst all. The most famous application for EEG is epilepsy diagnosis and monitoring [27] [37]. It is also used in diagnosis of coma, encephalopathy (syndrome of global brain dysfunction) , brain death and diagnosis of tumors, stroke and other focal brain disorders [33]. Prolonged multi-channel EEG recording is required for the evaluation of an epilepsy surgery candidate in order to define precisely the epileptogenic areas and determine the suitability of surgical

intervention [1]. It may also be used in assistive technology for paralyzed patients [54] [55]. EEG signals are also used in seizure prediction and detection [12] [61].

Although it was first introduced to service clinical needs, many Industrial fields have expressed great interest in using EEG signals in their products and some of these applications are listed below:

- Honda is attempting to develop a system to move its Asimo robot using EEG, a technology which it eventually hopes to incorporate into its automobiles [41].

Figure 1.3. **A Honda employee uses headgear to demonstrate technology that links human thoughts to robots from [41].**

- The Defense Advanced Research Projects Agency (DARPA) has budgeted $4 million in 2009 to investigate technology to enable soldiers on the battlefield to communicate via computer-mediated telepathy. The aim is to analyze neural signals that exist in the brain before words are spoken [43].
- Cathy Hutchinson, who suffered a stroke that left her paralyzed and unable to speak, is among the first humans to have her brain directly wired to a computer, Hutchinson volunteered to have the same kind of sensors used by

Andrew Schwartz, a neuroscientist at the University of Pittsburgh implanted into her motor cortex. By using only her mind, Cathy was able to control the movement of a cursor on the computer screen [52].

- Other applications include Games applications [44] [46] [45], Lie detection applications [42], speechless communications [54] [57] and remote control applications [53] [56].

1.3 Approach & Goals

In order to address the many limitations and constraints facing BCI data acquisition designs we will be focusing on five main issues and prospective solutions:

1) Noise, since the EEG signal is very susceptible to interference our goal is to ensure our system is highly robust against noise interference.
2) Low Power, ensuring the low power usage of our system is a main goal to support mobile applications.
3) Electrode Placement: We aim to support all types of electrodes available in the market especially dry electrodes to facilitate the electrode placement process.
4) Intelligent Control, Scalability and Modularity: We also aim to provide a totally flexible platform that is capable of adding any future modules or enhancement to serve the application needs and is equipped with smart control units causing the data acquisition process to be more efficient. It is also our goal to ensure the scalability of the design.
5) Flexibility and customizability: One of the main goals of our system is to provide researchers with a transparent interface to EEG signals, allowing them

to use our system in their different applications and easily interface it with their processing platforms.

1.4 Organization

The rest of the thesis is organized as follows: Chapter two contains the literature review of the problem and the methods and techniques of EEG data acquisition used in BCI designs. It also contains a representation of current solutions and explains how the state of the art designs address the issue.

Chapter three is an explanation of the system architecture of the proposed system listing its features and design parameters. Chapter four is a detailed elaboration of the prototype design specifying its engineering aspects, features and capabilities. Finally in Chapter five we discuss our conclusion and our suggested directions for future research.

Chapter 2

Literature Search

2.0 Overview

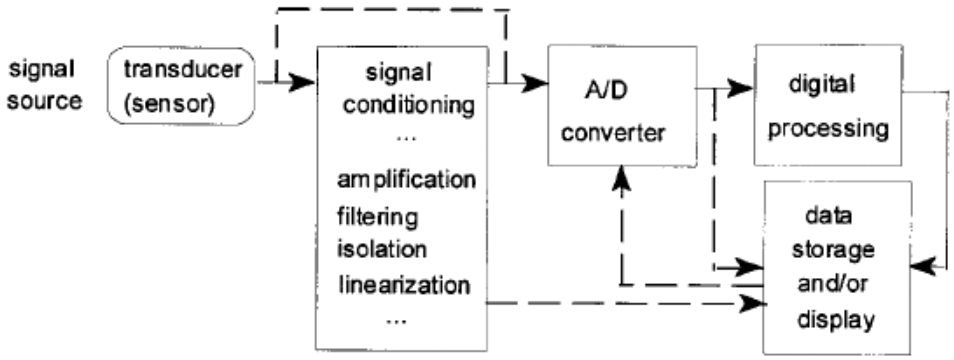
In this chapter we will discuss the BCI design concepts for EEG data acquisition, listing the different components and requirements for an acceptable BCI Design. Examples of existing BCI designs will be illustrated and discussed as well.

2.1 BCI Design and EEG Data Acquisition

Due to their extremely low amplitude [60] measuring EEG signals is not an easy task compared to measuring other noninvasive biosignals such as the electrocardiogram (ECG), electromyogram (EMG), and electrooculogram (EOG) signals [02] [59].

Taking the extremely sensitive nature of EEG signals into consideration, a BCI takes on the role of carefully gathering and conditioning brain waves information represented by EEG and recording it for further processing or analysis. A common data acquisition stage of digital EEG recording systems consists of three main stages [7] (see figure 2.1)

- EEG Electrodes (sensors).
- EEG signal Conditioning.
- Analog to Digital Conversion.



(a) (b)

Figure 2.1. **A typical EEG BCI design composed of (a) Data Acquisition stage and (b) Processing and storage stage from [7].**

In the Next section we will be elaborating on each of these stages' details and design aspects.

2.1.1 EEG electrodes.

2.1.1.1 ***Electrodes overview.*** The reliability signals extracted from bioelectrodes are of vital importance for medical applications such as EEG, EMG, and ECG. Bioelectrodes take on the role of converting the bipotential signals into measurable electrical signals.

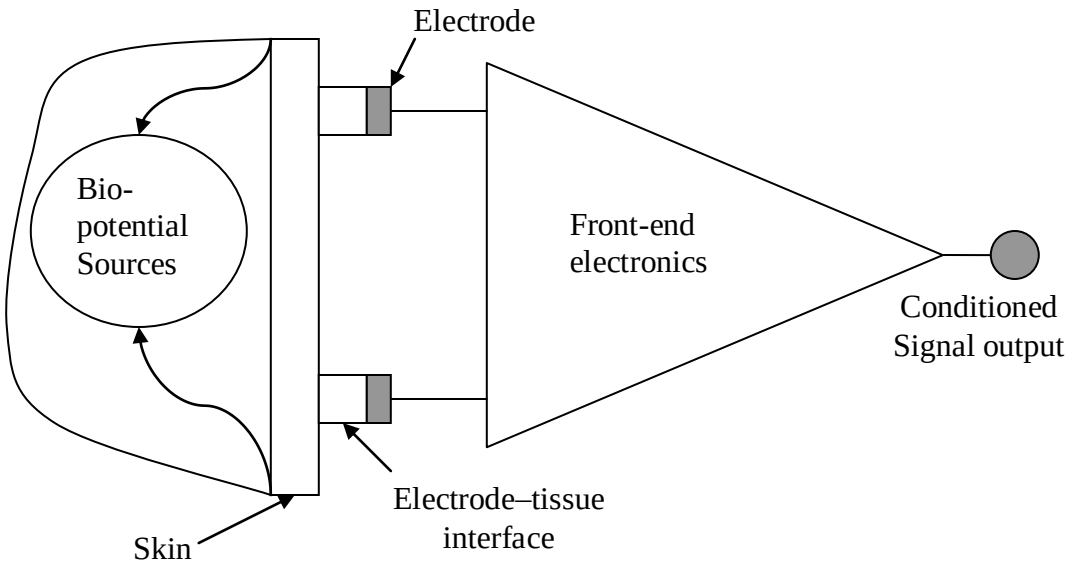


Figure 2.2. **Bioptential measurements using electrodes from [02].**

The most commonly used bioelectrode is the silver/silver chloride (Ag/AgCl) type [19], [2] which can be found in a reusable form and as a disposable electrode. Other Types of electrodes are also used in EEG applications to overcome the disadvantages of the common Ag/AgCl electrodes [3] [31].

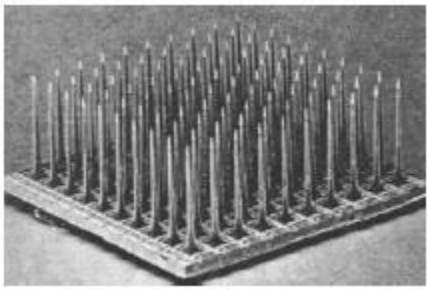
Electrodes can be classified according to their different characteristics:

- Electrodes' placement method: invasive or noninvasive [2] [22].
- Conductive Gel Requirement: wet or dry electrodes [19] [8].
- Skin Contact: contact electrodes or non-contact electrodes [17] [29].
- Active or inactive electrodes [20] [21].

(a) Ag-AgCl electrode

(b) Active electrodes

(c) Standard 256 channel EEG cap



(d) Intra-cortical electrode array

Figure 2.3. **Different types of EEG electrodes from [2].**

Commonly used electrodes require conductive gel placement in order to provide a good connection between the scalp and the electrode, the process of the gel application is a huge factor limiting the usage of EEG system [3] [35]. The gel takes a considerably long time to apply and dries after a certain period of time, thus other dry connection based electrodes are now being used in EEG data acquisition. This type of electrode does not need an extensive set-up time, and it is convenient for long-term recordings [16]. Examples of dry electrodes currently used are the Microelectromechanical systems (MEMS) based sensors [18] and active electrodes [20].

2.1.1.2 ***Electrodes placement.*** The most commonly used standard for electrodes placement is the 10-20 standard [2] [39]; this standard defines how the electrodes are generally placed and named (see figure 2.4). This system has been initially designed for 19 electrodes; however, extended versions have been proposed in order to deal with the larger number of electrodes [5].

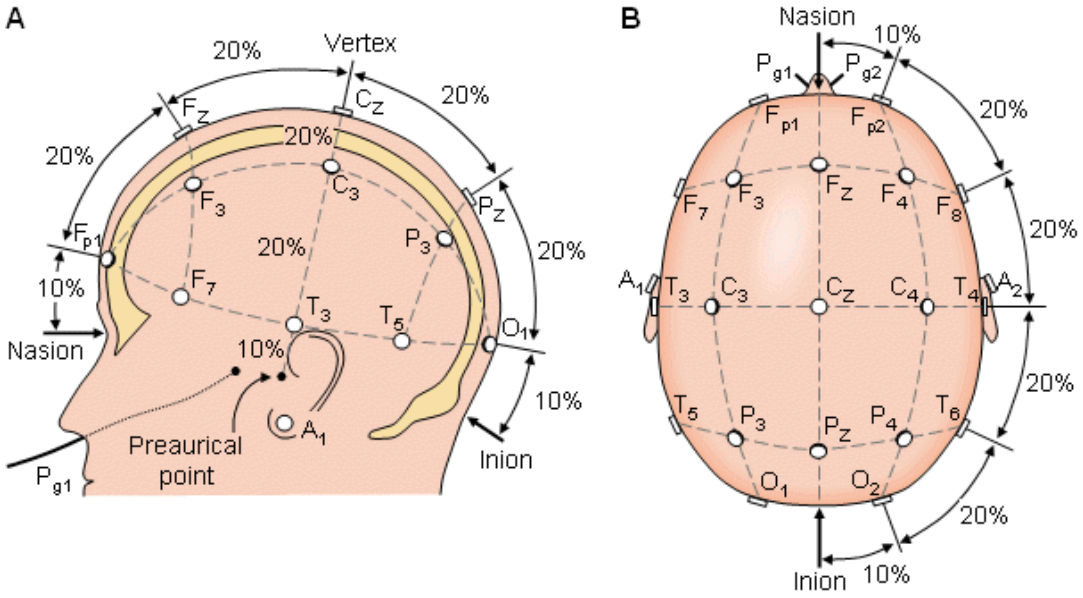


Figure 2.4. **Positions and names of the 10-20 international system electrodes from [49].**

EEG data can be gathered using a minimum of three electrodes: 1) sensor electrode, 2) the reference electrode and 3) the ground electrode. [58] The sensor electrode can be placed anywhere on the scalp according to the data required to be gathered, the reference electrode is used for noise cancellation and common mode rejection (CMR) [04] [58] and it is usually placed behind the ear where the least EEG

signals are normally located. The Ground electrode can be placed at any part on the scalp [58].

2.1.2 EEG signal conditioning. EEG signal conditioning is first accomplished by amplifying the micro volt range signal [7] into a much measurable signal by the analog to digital converter, then filtering takes place to reject the unwanted frequency ranges.

Bipotential amplifiers are required not to cause any influence on the monitored physiological process, it is also responsible of preventing distortion of the measured signal and providing the best possible separation between the signal and interference [13]. Figure 2.5 describes the different components of biosignal conditioning.

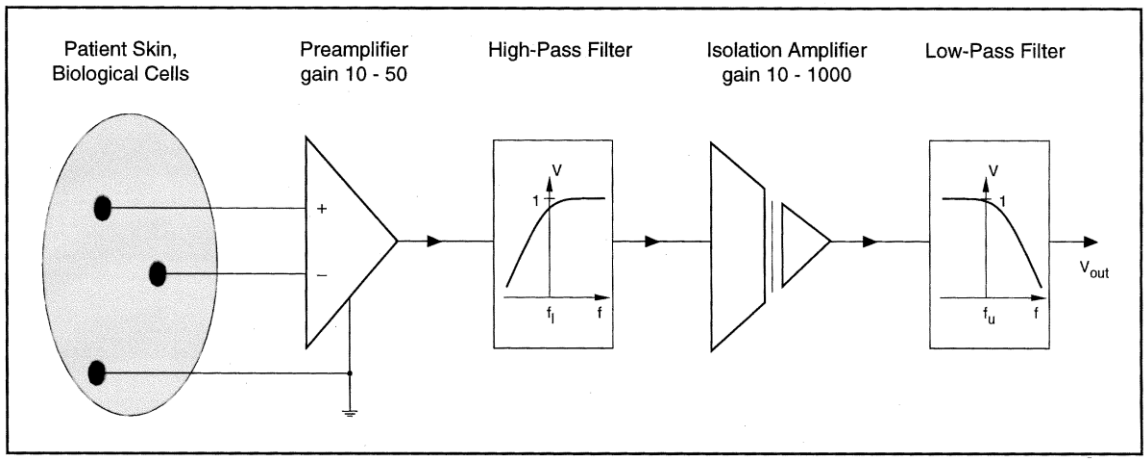


Figure 2.5. **EEG Signal conditioning from [13].**

The common mode rejection ratio (or CMRR) of an amplifier is defined as the ratio of the differential mode gain over the common mode gain [13]. It is critical for the CMRR to be as high as possible in biopotential amplifier to minimize the common mode interference effect on the signal. Another source of distortion that could be affecting the

biopotential signal is the impedance unbalance. Since source impedance unbalances of 5,000 to 10,000 Ω mainly caused by electrodes are not uncommon, and sufficient rejection of line frequency interferences requires a minimum CMRR of 100 dB. The input impedance of the amplifier should be at least 1000 MΩ at 60 Hz to prevent source impedance mismatch from decreasing the overall CMRR of the amplifier [13] [24]. State-of-the-art biopotential amplifiers provide a CMRR of 120 to 140 dB [13]. Equation 1, the amplifier transfer function [13], describes the output voltage in terms of the CMMR, amplifier gain, and input and source impedance.

$$V_{out} = G_D V_{biol} + \frac{G_D V_c}{CMRR} + G_D V_c \left(1 - \frac{Z_{in}}{Z_{in} + Z_1 - Z_2} \right) \quad (1)$$

Where:

V_{out} = Amplifier Output voltage G_D=Amplifier Gain

V_{biol} = biopotential input voltage V_C= common mode signal

Z_{in} = input impedance Z_1, Z_2 = Source impedances

CMRR = common mode rejection ratio

Signal to Noise Ratio (SNR) is another parameter to be taken into consideration when designing a biopotetial amplifier. High SNR requires the use of very low noise amplifiers and the limitation of bandwidth. Current technology offers differential amplifiers with voltage noise of less than 10 nV/√Hz and current noise less than 1pA/√Hz [13].

Filtering EEG input signals is a definite requirement in order to gather the required EEG frequency range only; a band pass filter is usually used with a 1-100 Hz

pass band [4]. Filtering also eliminates interference signals like electrode half-cell potentials and preamplifier offset potentials and reduces the noise amplitude by limiting the amplifier bandwidth. Active Bessel filters are the preferred filter types due to their smooth transfer function [7] [13]. Digital filters might be used for elimination of the electromagnetic or electrostatic interference arising from the presence of 50 or 60Hz line current, this is typically done using a notch filter to attenuate this noise signal [7] [3].

2.1.3 Analog to digital conversion. EEG signals are analog signals and to process them digitally an Analog to Digital Converter (ADC) is used. The analog-to-digital converter stage is the last link in the chain between the analog domain and the digitized signal path. As mentioned earlier, noise is a main concern in EEG data acquisition. It is a must for the ADC used to comply with the low noise requirements. Data acquisition systems that use differential ADCs are increasingly common because of both their improved interference rejection capability and their larger dynamic range in low-voltage circuits as in the case of portable systems [30].

Sampling frequency is not a major concern since only the 1-100Hz EEG signal range is targeted. The common sampling frequency range is 256–512 Hz in clinical scalp EEG. Sampling rates of up to 20 KHz are used in some research applications [33].

2.2 Survey of Current Solutions

EEG data acquisition has been presented and investigated in many studies, patents, published articles and products; in the next section we will be conducting a survey of these solutions describing their theory of operation, specifications, advantages and disadvantages.

2.3 Published Research Articles

2.3.1 Low noise multichannel amplifier for portable EEG biomedical applications. In [01] a multiple channel biopotential amplifier is proposed. It applies the conventional design for biosignal acquisition systems where it is composed of a low pass filter, an instrumentation amplifier, and a high pass filter. Its amplification gain is 1 million. The EEG data is sampled at 128 samples per second and its filtering pass band is 0.5 - 35 Hz, therefore this system is not suitable for EEG signals of frequency more than 35Hz such as the Gamma signals [23].

The system supports portable applications and could be battery operated. It is also interfaced to a microprocessor circuit that stores the recorded EEG data in a Personal Computer Memory Card International Association (PCMCIA) memory which can store EEG signals from up to sixteen EEG channels during a 24 hours session. Figure 2.6 shows the overall architecture of the system proposed in [1]. Wavelet compression is used to improve the storing efficiency of the data and to increase the number of signal channels to be recorded.

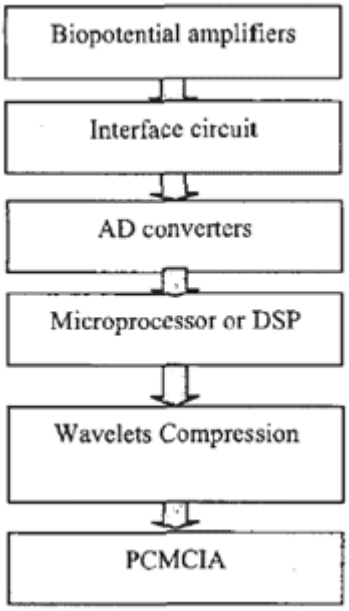


Figure 2.6. **A multichannel EEG recording system from [01].**

Since this system stores the recorded EEG data into a PCMCIA memory, so it is not designed for real time data transfer and doesn't support ,

2.3.2 A brain-machine interface using dry-contact, low-noise EEG sensors. Another BCI design is proposed in [3] that is based on the same authors' previous research [4]. This proposed system provides a non-expensive BCI design that attempts to solve two main limitations of EEG BCI data acquisition systems which are the conductive gel requirements for electrode and the immobility due to high power consumptions.

This design only consumes 3mW of power and limits the amount of wiring by daisy chaining the data acquisition nodes together and the final data collected is a concatenation of all the readings of sensors combined which in our opinion is a valuable

addition to EEG recording systems that solves the wiring obstacles but may introduce latency to the system and prevent the user from accessing each single electrode's data individually. In our system we intend to introduce granularity to the sensor addressing scheme, where as the user will be able to communicate with each electrode individually without any dependency on the other electrodes or acquisition nodes.

The front end design is constructed of inexpensive components; the mid-band gain is 1000 (60dB) with noise filtered out below 1 Hz and above 100 Hz. The analog to digital sampling rate used is 2KSPS. Figure 2.7 shows the front end schematic of the system. It is to be noted that the pin layout of the 6010 Operation amplifier (OpAmp) stated in the schematic doesn't match the true pin layout of the 6010 OpAmp [48] Also it is not mentioned if the shutdown capability of the 6010 OpAmp is utilized which would affect the power consumption efficiency greatly.

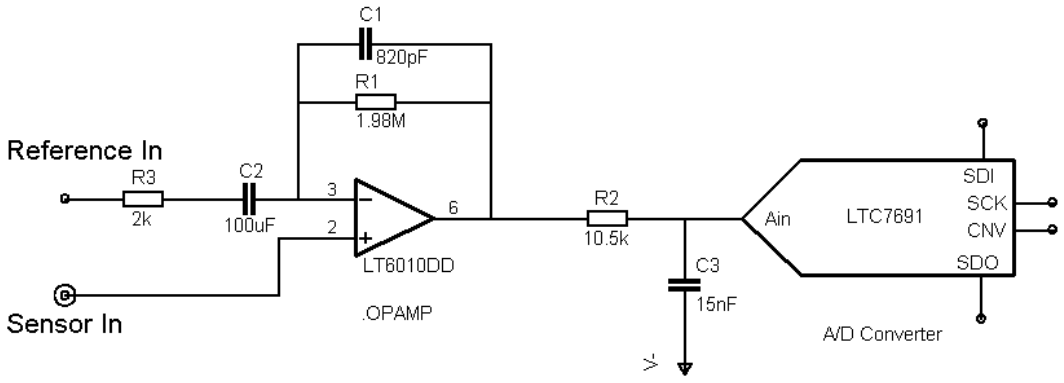


Figure 2.7. **The BCI front end schematic from [3].**

The system uses seven sensors where sensor 7 was used as a reference and was placed behind the ear where the least EEG signal can be detected; the EEG signal

gathered from the remaining sensors is subtracted from the reference sensor's signal eliminating the common noise effect. It was found that the further the sensors are from the reference the more noise levels are in the signal gathered. A notch filter was implemented in the software to reject the power line interference.

The MEMS based sensors used by the system provides an important solution to the gel application issue in the case of wet electrodes however MEMS based electrodes can only be applied to scalp areas with no hair where wet electrodes must be used for reliable data acquisition. The system does support both dry and wet electrodes inputs. Figure 2.8 shows an image of the designed system mounted on a baseball cap where the electrodes are to be attached to the subject's forehead.

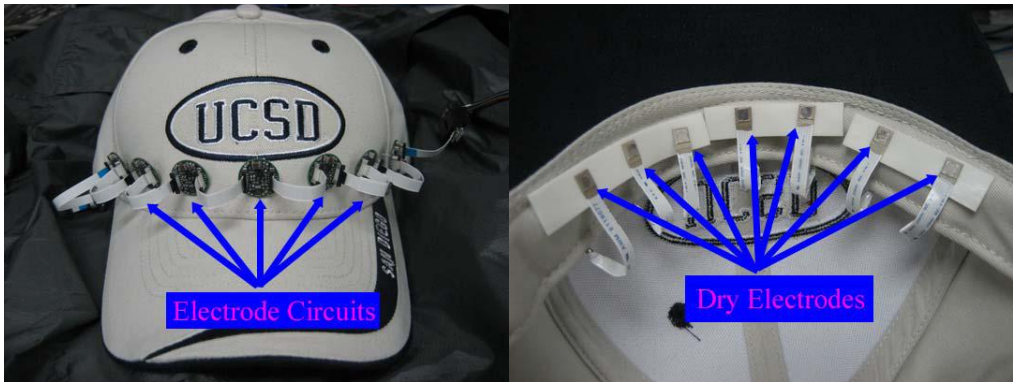


Figure 2.8. **The BCI system using dry EEG electrodes from [3].**

2.3.3 Epileptic seizure prediction using EEG. In [12], EEG recording was utilized for Epileptic seizure prediction, it used the Nicolet 5000 video EEG acquisition system which contains a 12-bit resolution analog-to-digital converter and sampled at a rate of 200 Hz with band pass filter settings of 0.1–100 Hz. Subdural (under the skin) strip electrodes were used and patients ages between (21-53) where hospitalized 3-14

days and continuous EEG monitoring was performed for epileptic surgery evaluation. This system outlines the urgent need for mobile EEG recording systems where epilepsy patients for example can be monitored without being hospitalized for prolonged periods of time, where as our mobile system will provide real time analysis support without eliminating the need for long recording periods.

2.3.4 A portable EEG recording system. A Portable EEG recording system is proposed in [15], the system uses gold-plated, cup type electrodes placed in bipolar arrays on the scalp following the standardized international 10-20 System [49]. The amplification is done through two stages, the first is using a preamplifier with very low noise differential JFET input to reduce high electrode source impedance the preamplifier gain is 100 and has a high CMRR (>120dB). The second amplification stage is done using two amplifiers the first is an isolation amplifier one with a constant gain of 10 and the second has a variable gain raging from 26-51 resulting in an overall system gain range of 25000 -51000. The band pass filtering range was between 1-25 Hz, in this system the data was recorded in an analog format on a miniaturized 4 channel FM tape recorder for further analysis**.**

2.3.5 A mobile EEG system with dry electrodes. Another EEG recording system is proposed in [16] that is designed for mobile applications. This design aims at providing an easy to use and wearable BCI-system. The system is composed of three main elements:

(1) An ultra-high input impedance bioamplifier.

(2) New dry electrodes suitable for long-term recording in real environments.

(3) Wireless connectivity using a low-power ADC equipped with a Bluetooth module.

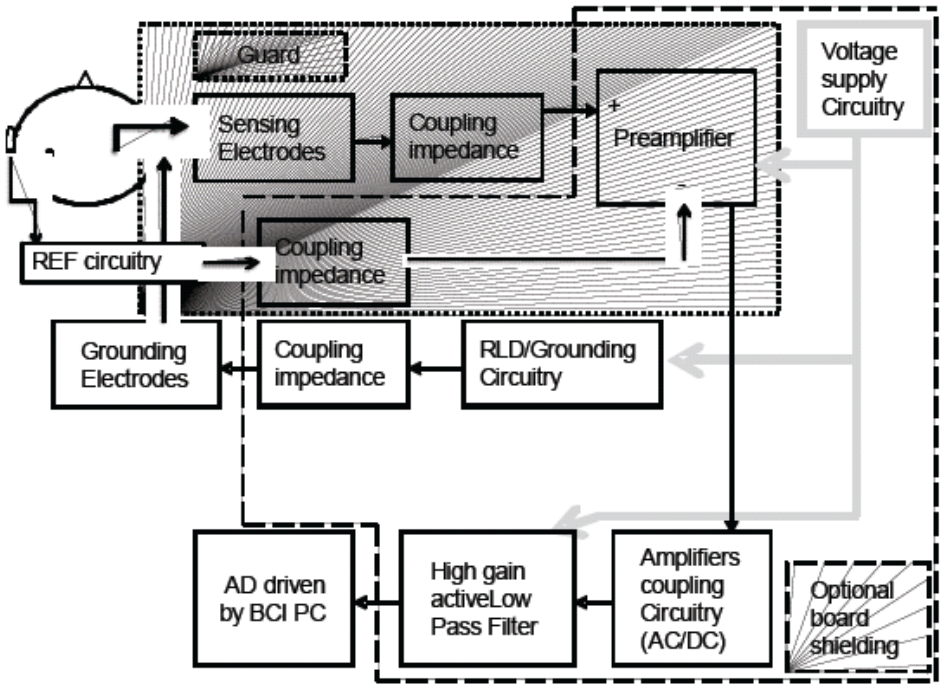


Figure 2.9. **Block diagram for the mobile EEG system from [16].**

This system is battery powered and the acquired data is transferred to the PC using bluetooth. A preamplifier of variable gain is applied to input signal where the gains varies according to the used electrodes (a gain of 6000 for use with dry electrodes and 50000 for golden and Ag/AgCl electrodes. The measured noise was less than 2 μV peak-to-peak in the bandwidth up to 10 Hz.

The band pass filter is tunable to provide a dynamic range serving the need of the application, the low pass filter is tunable up to 5 Hz cut off frequency and the high pass filter is tunable to a maximum of 100 Hz cut off frequency.

A new kind of dry passive electrodes is proposed and used. These electrodes are fabricated with commercially available 1.5 mm thick silicone conductive rubber shaped in discs of 8 mm diameter (see figure 2.10). The ADC sampling rate used was 256 SPS with a 12-bit or 16-bit resolution. However in our system we will support higher sampling rates (up to 23 KSPS) and higher resolution (24-bit).

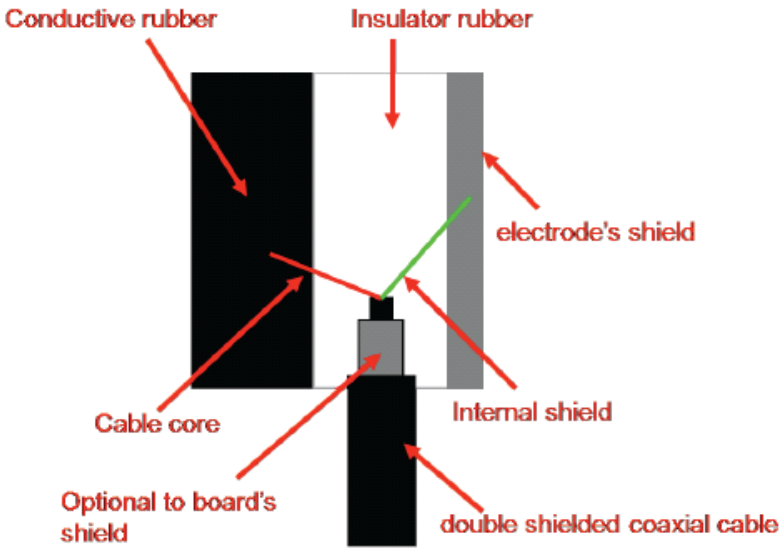


Figure 2.10. **Dry passive electrodes from [16].**

2.3.6 Micropower active non-contact EEG electrode. A similar approach to the system proposed in [3]; another low power mobile design is introduced in [17]. This design proposed a new active non contact capacitance based electrode. Each sensor (see figure 2.11) consists of two small rounds electrically connected standard printed circuit boards (PCB). The bottom board is the size of a US quarter and contains the sensing plate along with the analog amplifier electronics. The top board, which is the size of a US nickel, contains the ADC and digital data interface.

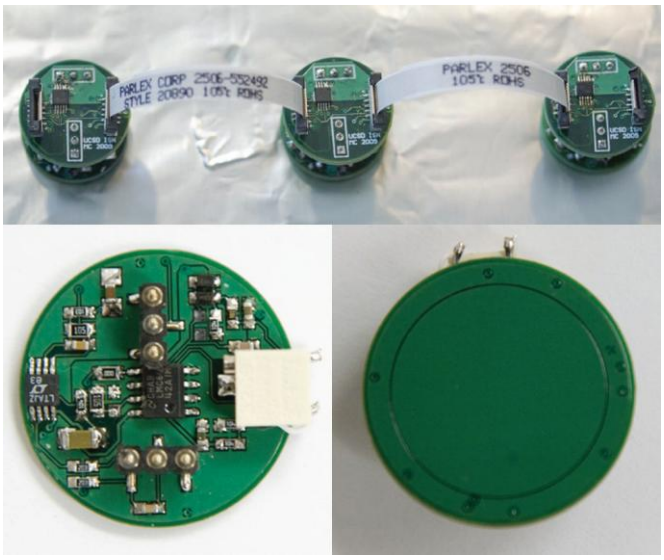


Figure 2.11. **Micropower active non-contact EEG electrode from [17].**

The Amplifier circuit consists of two stages the first has a gain of 11 followed by a differential amplifier with a gain of 100 producing a total system gain of 1100. The used LMC6442 operational amplifier has a very low current noise (0.2fA/√Hz). In addition, its power consumption is extremely low – 1μA per channel.

The Analog to digital converter used is a 16 bit resolution and its output is daisy chained in a serial connection which connects to a custom USB data acquisition interface.

2.3.7 EEG data acquisition system for measurement of auditory evoked potentials. In [28] an EEG data acquisition system is proposed to aid in conducting necessary hearing diagnostic tests during the first 3 to 6 months after a child's birth to help diagnose level of hearing impairment of patients. It utilizes the EEG measurement equipment with Evoked Potentials analysis capabilities to assess the brain activity due to external auditory stimuli.

The data acquisition system proposed in this paper consists of:

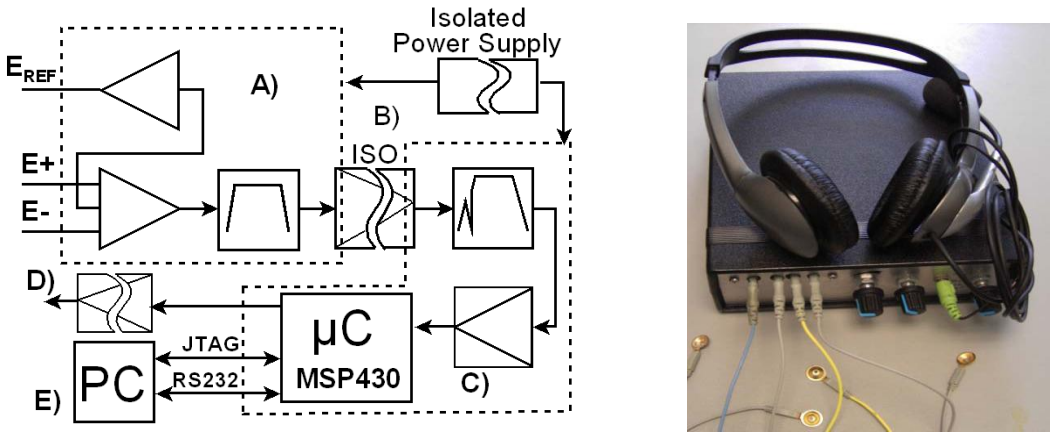
a) A three electrode scheme for measuring EEG signals.

b) Isolation power supply and coupling amplifier.

c) Signal conditioning and digitizing section.

d) Auditory stimuli generation section.

e) Communication with a host PC for programming (JTAG) and data transfer (see figure 2.12).



(a) EEG data acquisition block diagram (b) EEG system proposed

Figure 2.12. **Evoked potentials EEG data acquisition system from [28].**

Amplification of the EEG signal takes place using an instrumentation amplifier with a CMMR larger than 110 dB. The signal is sampled at a rate of 47Ksps (Kilo Sample per Second) with 12 bit resolution. The data acquisition process results in a set of 800 12-bit values which are averaged with the next data set, to produce the EEG auditory evoked potential measurement. The number of times the process is repeated is controlled by a C++ program residing in the host computer. The data acquired is transferred to the host pc using a standard serial RS232 interface. The RS232 connection was tested successfully with USB interface connections as well. This system can also be operated by a 9V battery.

2.4 Patents

2.4.1 Communication using brainwaves. U.S. Patent referenced by [51] describes a BCI system capable of utilizing the mu rhythm EEG signals to communicate with the environment, a 64 channel BCI system is designed and a 64 differential amplifier is used for signal analysis.

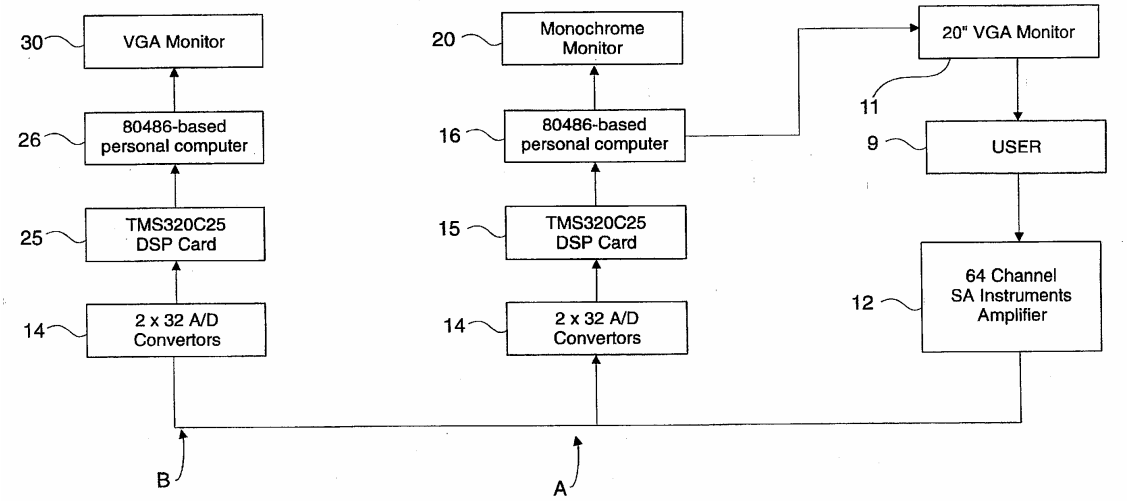


Figure 2.13. **BCI system block diagram from [51].**

The EEG signal is analyzed using a digital signal processing card (TMS320C25) and then according to the analysis result feedback to presented to the user through a monochrome or a Video Graphic Array (VGA) monitor.

2.4.2 Brain computer interface. In U.S. patent [38] a brain computer interface is described responsible for analyzing EEG signals acquired using subdural electrodes and interfacing the output to a desktop computer for example to move the cursor. Figure 2.14 shows the block diagram of the proposed system.

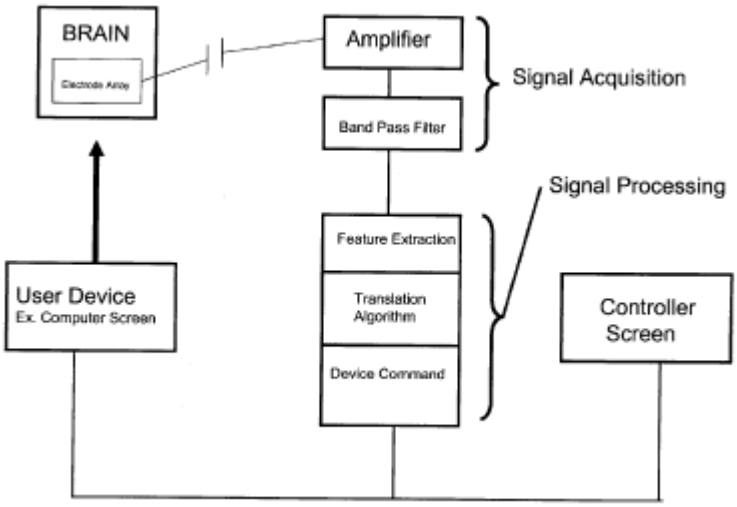


Figure 2.14. **Block diagram of a BCI proposed by [38].**

2.4.3 Ceramic single plate capacitor EEG electrode. In [11], this U.S Patent introduces a dry capacitive ceramic EEG electrode composed of a very thin metal disk that is housed between two relatively thicker layers of ceramic. The electrode has an amplifier PCB circuit attached to it for EEG signal conditioning.

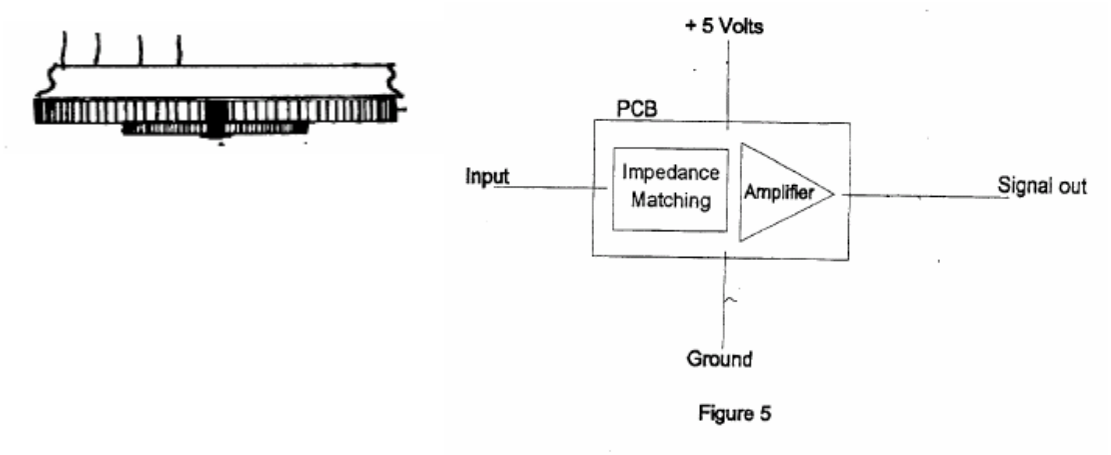


Figure 2.15. **Ceramic EEG electrode from [11].**

The proposed ceramic electrode doesn't require abrasive material or conductive gel with minimized chances of patient being shocked due to it high insulation.

2.4.4 Real time EEG spectral analyzer. U.S. Patent referenced by [10] describes a design for analyzing the EEG signals in real time; it divides the frequency bands of the EEG signal into 4 bands at each channel and frequency ranges are compared to predetermined base line values and audible or visual alerts are initiated.

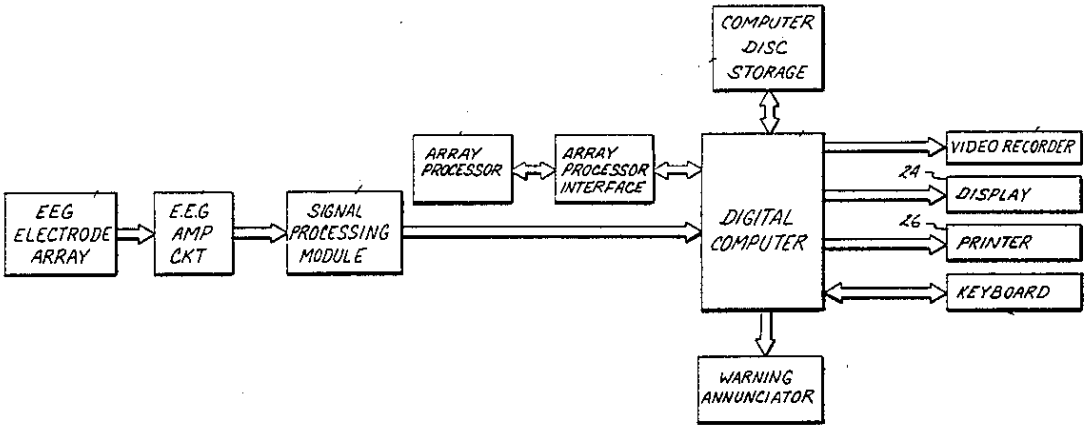


Figure 2.16. **Real time EEG spectral analyzer from [10].**

The EEG signal is sampled with a 256 SPS rate. The data is then written to a random access memory (RAM), the array processor converts the digitized signals from the time domain to the frequency domain .The digital computer then analyzes the data and initiates the warning through the warning annunciation methods when certain values are reached.

2.5 Commercial Products

There are multiple EEG data acquisition based products in the market however the underlying theory of operation is not stated in details within the product specifications. In the next subsection we will be listing some products that deal with EEG data acquisition.

2.5.1 OCZ neural impulse actuator. OCZ introduced the neural impulse actuator [62] which is product capable on translating EEG waves into certain computer commands on a desktop computer.

Figure 2.17. **Neural impulse actuator from [62].**

It is interfaced through the USB connection, it used in games, reducing reaction times and animation creation.

2.5.2 Intendex. In CeBIT 2010 the word largest computer expo, the first commercial BCI was introduced [63], intendex from guger technologies allows user to type using only their thoughts.

Figure 2.18. **Intendex, the first commercial BCI system from [63].**

Priced at $12,000, this BCI device connects the user's brain waves through a standard EEG cap, and by focusing on the letters displayed on the computer screen. The user's EEG signal received from the cap is analyzed and the intended letter is chosen, Intendex is capable of operating at speeds as fast as one letter per second.

2.6 Current Solutions Survey Conclusion

It is clear from the current state of the art solutions and products stated in this chapter that none of them provides an open customizable platform to be managed by the researchers. Most of the existing BCI designs are custom built for specific applications. Thus in our design we will be exceeding or at least matching the state of the art specifications of BCI design. We will also ensure that our system is flexible and could be

tailored by the EEG application developers according to their requirements. Also it will support the most current communication interfaces allowing researchers to connect their processing platforms to our system seamlessly.

Chapter 3

System Architecture

3.0 Overview

In this Chapter we will discuss our system architecture design for an intelligent data acquisition system suitable for EEG applications that will serve researchers' needs and act as a part of a development platform for EEG signal analysis and applications. We will also discuss the design details and features' specification and compare our design to previously discussed systems.

3.1 System Requirements and Specifications

The system requirements are the set of minimum prerequisites that the design must meet. This could be the boundary values permitted for the power, weight, size and noise levels. In the following sections we will provide a description of the features and specifications of our novel design for several aspects of the design including special considerations on noise levels, power consumption, mobility, size, weight, input signals supported, and interoperability with different interfaces.

3.1.1 Size. In order for the design to support mobile operation the size should be as small as possible. This is also required in case the designed system is to be mounted on certain head gear or cap to ease usability. Our intended design outer

dimension size is approximately 20 squared inches in area and 1.25 inches of height (see figure 3.1).

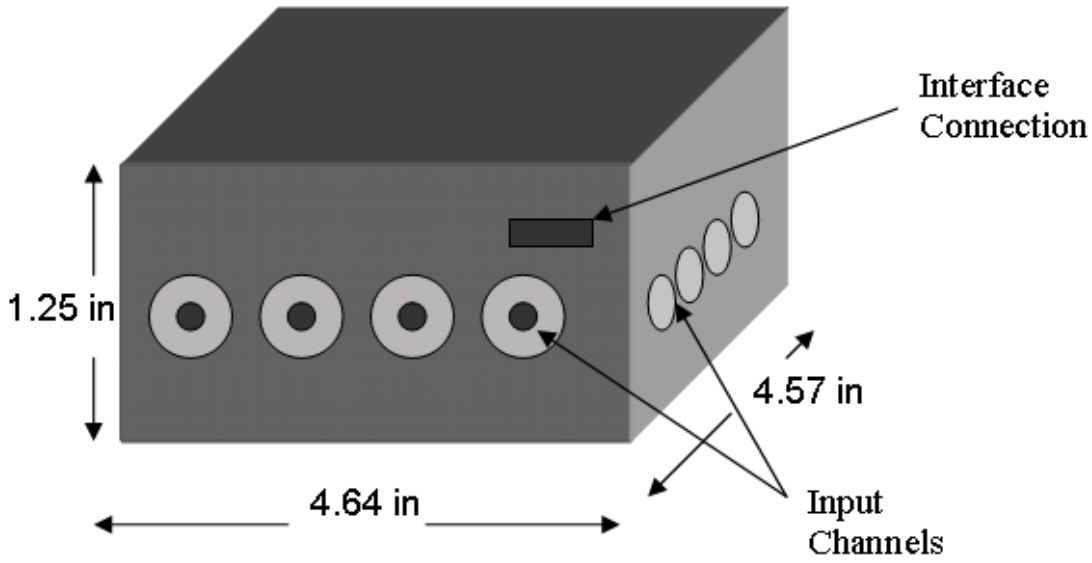


Figure 3.1. **System physical design structure**.

3.1.2 Weight. Weight is an important factor when designing portable systems. Our systems' weight is not of a large concern due its relative small size. The weight is expected be approximately 30 gm. Thus the system should be very suitable for mobile applications.

3.1.3 Inputs. Our proposed system supports up to 16 channels of input signals which is sufficient for various research and consumer applications. It is designed to support most commonly used EEG electrodes such as conventional wet electrodes and novel dry electrodes such as MEMS based electrodes.

3.1.4 Power consumption. One of the main design goals is to support low power operation, thus the designed system current consumption rate is less than 100mA and this will be further explained later in following sections of this chapter. This low power design allows the system to be easily incorporated in portable applications that require battery operation.

3.1.5 Noise levels. Since signal interference has a great impact on any EEG data acquisition system, especially on the analog component of the design we comply with the state of art noise requirements of having a high amplifier CMRR (no loss than 120 dB) we also support high SNR of at least 100dB.

3.2 System Overview and Theory of Operation

Our proposed system design specifications match the EEG data acquisition requirements such as the EEG electrodes compatibility, low noise, and capability of mobile applications. Our design also supports low power operation for battery operated applications. Our design is composed of three main elements:

1. Analog Front End: this component is responsible for conditioning the input EEG signal by performing signal amplification, filtering and noise elimination.
2. Analog to Digital conversion: and this unit takes on the role of converting its analog input from stage one to a digital signal to be processed or stored according to the application.
3. Digital control and processing: this is carried out by a microcontroller circuit that orchestrates the overall data acquisition process and connects the system to other compatible interfaces.

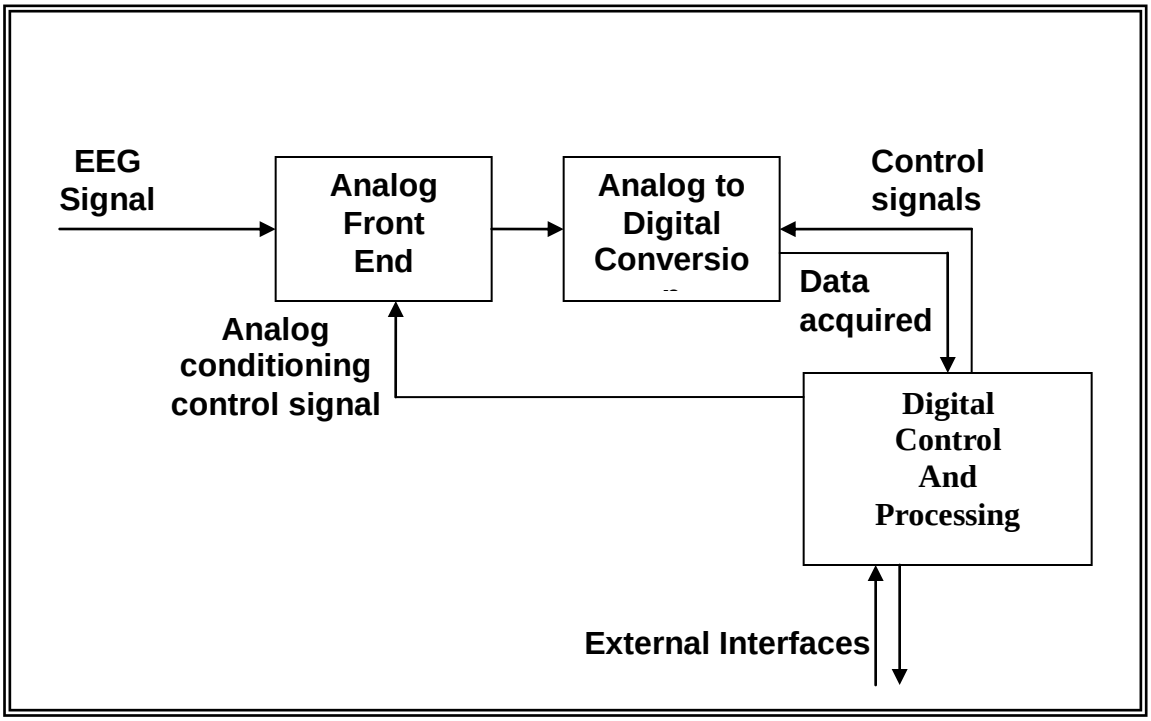


***Figure 3.2*. Block diagram of the overall architecture.**

In the next sections we will be explaining in details each of the design components listing its specifications and capabilities. We will also be explaining the flexibility of these components and their possible applications.

3.3 Analog Front End (AFE)

As we have mentioned before, this stage is responsible for conditioning the EEG signal input by filtering and amplification, it is also clears the input signal from interference and noise in order to provide a reliable and measurable signal to the ADC.

The proposed front end Block diagram is shown in figure 3.3. This circuit takes two inputs 1) the input EEG electrode 2) the reference electrode. These inputs are transferred to the Operational Amplifier (OpAmp) in order for the differential amplification to take place. A band pass filter is also applied to limit the frequency to the

desired range. Other circuits are also added such as the Null and the shutdown circuit. In the next subsection we will elaborate on each element of this design.

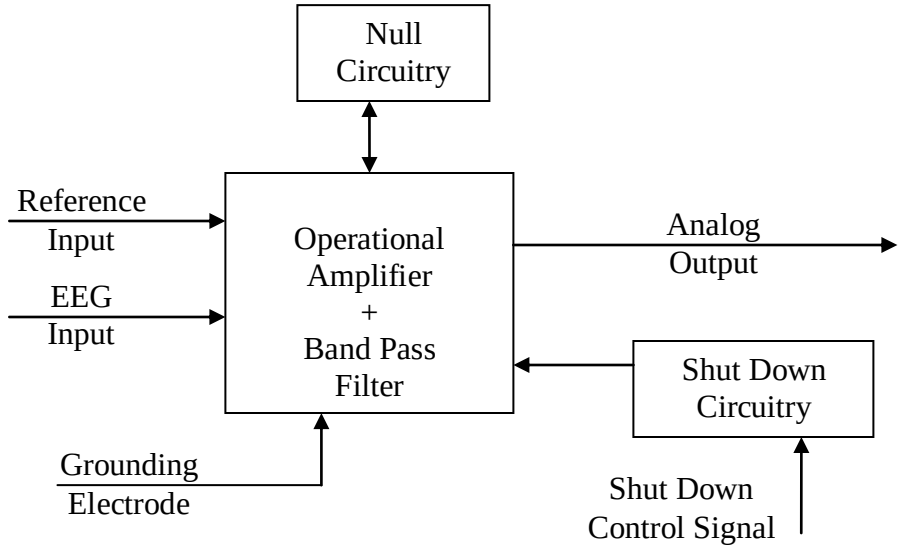


Figure 3.3. **Analog front end block diagram.**

3.3.1 Input electrodes. This design supports both dry and wet electrodes, as shown in figure 3.3 each channel requires a minimum of three EEG electrodes in order to acquire data. First the EEG input electrode which carries the targeted signal and is to be placed according to the international 10-20 electrode placement system [49]. The second electrode is the reference and is to be placed behind the ear where the least EEG signal can be found and this signal is used for noise cancellation. The third and last electrode is the ground electrode and it is the reference voltage to which all the other EEG electrode potentials are referenced. It is usually placed in the middle of the forehead and it is directly connected to the analog ground of the circuit.

3.3.2 Amplification and filtering. The amplifying and filtering part of the circuit is achieved using an operational amplifier based design similar to the analog front end circuit of [3] &[4] which was discussed in chapter 2 section 2.3.2.

The chosen operational amplifier is the LT6010 which is a low power, low noise, precision, and rail-to-rail operational amplifier. It only draws 135µA of supply current on a 5 v supply and it has a CMRR of 135dB [48]. Its 14nV/√Hz input noise voltage is extremely low making it perfect for our application where noise and power are huge concerns. Also it is available in relatively small packages (3mm by 3mm) which make it very suitable for mobile applications.

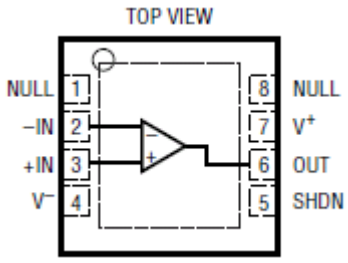


Figure 3.4. **The LT6010 top view (DD package) from [48].**

The amplifier gain value is approximately equal to 1000 (60dB) ; it can also be changed if needed by adding flexibility in the printed circuit board layout which will be explained better in later chapters. The Band pass filter is composed using a single OpAmp based filter design with a pass range of 1-100 Hz.

3.3.3 The null circuit. In case of impedance mismatch, offset voltage might be produced. This offset voltage can create offsets or drifting in the operational amplifier. Therefore, the null circuit was put in place. Using the null feature of the selected LT6010

OpAmp, this null process is done by applying a short circuit on the two input of the OpAmp and adjusting the value of the resistance across the null inputs of the OpAmp until the output is zero, this will ensure that the offset voltage effect on canceled.

3.3.4 The shutdown circuit. The shutdown feature included in the LT6010 OpAmp plays a vital role in managing the power consumption effectively. The LT6010 draws only 12μA at shutdown compared to 135μA at operation. Therefore the shutdown signals are controlled by the Digital control and processing unit to only turn on the channel amplification when needed.

3.4 Analog to Digital Conversion

Although the analog signal going into the analog to digital conversion is a much cleaner and noise resistant than the system's EEG input signal, low noise condition must still be taken into consideration when designing a the ADC part of the system. Figure 3.5 describes the block diagram of the proposed ADC module design.

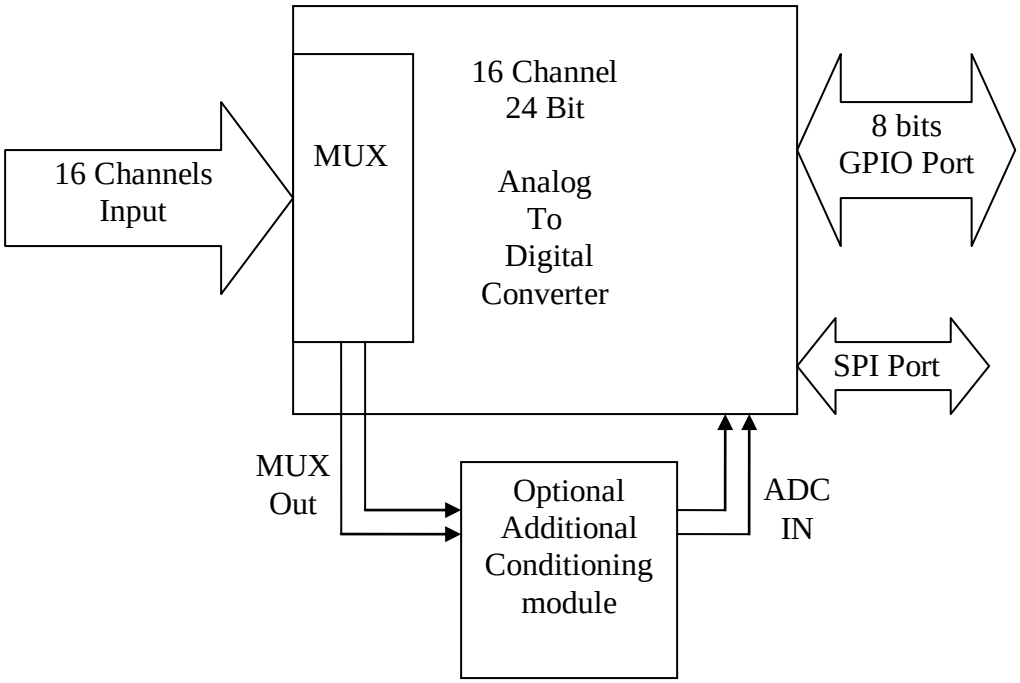


Figure 3.5. **Proposed ADC module design.**

The chosen ADC chip is ADS1258; it is 16 single ended / 8 differential inputs, 24 bit resolution analog to digital converter [26]. It only consumes 42mW of power and its noise rating is 2.8µVrms at 1.8KSPS. In the next subsections we will be focusing on key issues in EEG data acquisition and how the proposed ADC design deals with them.

3.4.1 Sampling rate. The ADS1258 is capable of sampling rates up to 23.7KSPS, and since most of the state-of-the-art EEG data acquisition system operate using sampling rates less than 2KSPS, the proposed ADC's sampling rate is more than sufficient for EEG application. However it is recommended to operate the ADC on low sampling rates, which will help reduce the amount of power dissipated unless otherwise required.

3.4.2 ADC multiplexed input. Multiplexed input is a feature included in the ADS1258 making it possible to further condition the input signal individually by placing additional conditioning circuitry between the available multiplexer output and the ADC input of the ADS1258. This is a great advantage in case additional filtering or voltage gain is required and it can be controlled through software communication with the ADC chip.

3.4.3 Sampling clock source. The ADS1258 chip gives us the option of using its own clock generated by the connected 32.7 KHz crystal or using an external source for the clock, we used the ADC clock instead of applying it from an external source in order to reduce the overhead on the processor and eliminate any additional sources of interference that might affect the circuit.

3.4.4 ADC interface. The ADS1258 uses the Serial Peripheral Interface (SPI) for data communication acting as a slave to the processing unit. All the control and data signals transferred between the ADC and the processor go through the SPI interface. The ADS1258 is also equipped with eight General Purpose Input output (GPIO) pins; these pins will be connected to a fast input/output port in the processor.

3.4.5 ADC bit resolution. The proposed ADC system has a resolution of 24 bits, although the maximum resolution we have seen in state of the art designs discussed earlier was 18 bits [4], however we have seen that it is recommended to have a higher resolution analog to digital conversion system. This will ensure early saturation due to eye blinks and other artifacts is prevented.

3.4.6 ADC design independence. The proposed ADC design is intended to be independent of the other components of the system; it could also be used in any other

data acquisition systems. This adds great flexibility to the design making it available for use in other application in need of a state-of-the-art analog to digital conversion module.

3.5 Digital Control and Processing Stage (DCP)

This stage is the brain of the whole system; it oversees the overall operation, controls the different components and acts as the interface to the outside world. The processing unit is based on the MCF51JM128 ColdFire microcontroller which is a member of the family of 32-bit reduced instruction set computing (RISC) microprocessors [25].

3.5.1 Processor features. The MCF51JM128or the JM microcontroller is a perfect fit for this data acquisition system it supports multiple interfaces such as the Universal Serial Bus (USB), Inter-Integrated Circuit (IIC), Universal Asynchronous Receiver/Transmitter (UART) and SPI which is required in order to communicate with the ADC module.

The JM micro also supports low power operation allowing it to operate from an external power source or through the standard USB port. It is also small in size which suits the mobile operation concept .It adds great flexibility to the overall system making it customizable according to the user's needs.

It could also perform processing duties such as filtering and minor data analysis but user should be aware of the limited digital signal processing capabilities of the JM processor due to its RISC based architecture. Code development for the JM microcontroller is commonly done using the Freescale CodWarrior software. It provides great support for the Freescale microcontrollers' platform development and provides many ready to use software modules

3.5.2 DCP and the ADC. The processor controls the analog to digital conversion through the SPI interface as mentioned earlier. It sends the commands initiating the conversion of the intended channel and waits for the data to be ready. It specifies if the signal is to be further conditioned using the additional conditioning circuitry located between the ADC's Multiplexer and the ADC input.

The DCP unit also sends control commands monitoring the state of the ADC and checks if any unexpected conditions are met and acts upon it. It also connects to the ADC through the 8 GPIO pins using Port A of the JM micro which is rapid general purpose input port for fast communications.

3.5.3 DCP and the AFE. The only communication that would occur between the processing unit and the analog front end (AFE) is the shutdown control signal; this signal is controlled by the JM micro using the other SPI interface. The shutdown SPI signal is transferred from serial data to parallel using shift registers allowing the JM microcontroller to control the shutdown condition of 16 channels using only the 2 pins of the SPI port. Figure 3.6 describes the communication between the DCP and the AFE.

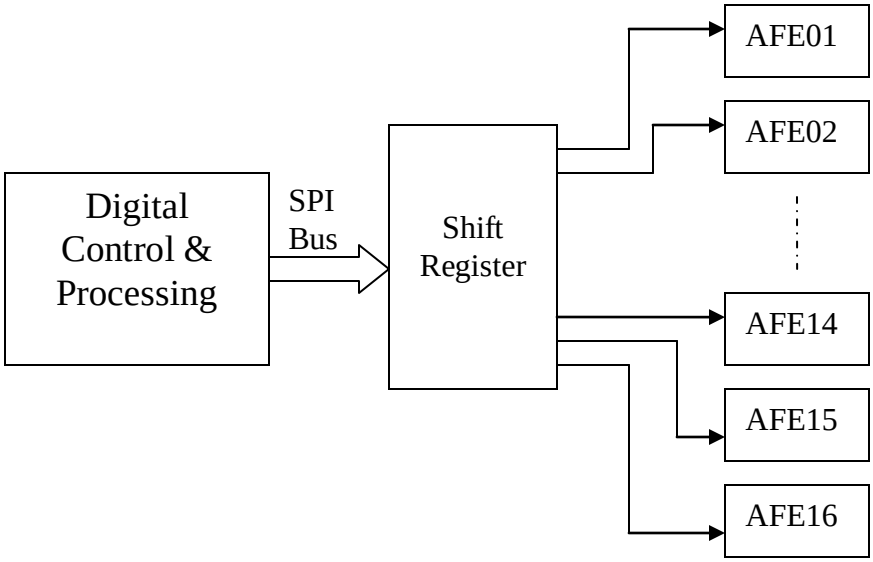


Figure 3.6. **Block diagram of the communication between the DCP and the AFE modules.**

3.6 Power Supply

Due to mobile requirements of the system; a flexible power supply design is recommended and thus provided by the Computer Group, a local embedded design company in south Florida. This Power supply design provides a battery operated system with a 9v rechargeable lithium battery, if the power supply is connected to an external source the battery will be in the charging state and if the external source is disconnected, the battery takes control and operates the system.

3.7 Modes of Operation

Because of the multi-featured processing unit; the proposed system supports three types of operation:

1) Stand alone operation mode.

2) Slave (interface) mode.

3) Intermediate processing mode.

In the following subsections we will further explain each of these modes.

3.7.1 Stand alone operation mode. In this mode the processing unit manages the data acquisition and carries on processing tasks as well. No other processor is present and all the analysis and processing is done by the DCP unit.

An example of applications operating in this mode is a simple EEG monitoring system where the processor acquires the EEG data and analyzes it using certain algorithms to distinguish between different EEG bands and certain actions are taken if the targeted bands reach a preset threshold values. For instance this could apply in the case of patient monitoring.

3.7.2 Slave (interface) operation mode. This mode is used when the user doesn't require any processing to be done by the DCP unit and the entire processing load is taken care of by external digital signal processors. In which case, the DCP unit only acts as a data acquisition manager waiting for commands from the master processor and executing them accordingly.

An example where this mode would be applicable is precise real time data analysis application where the DCP unit is incapable of carrying out such processing and is used only for high data transfer.

3.7.3 Intermediate processing mode. In this mode the processing tasks are divided amongst the DCP and the external processor, this occurs in case the external processor demands the DCP to perform preprocessing functions such as digital filtering for example.

An example for the use of this mode is when the external processor requires only a certain band of EEG frequencies to be input to it so the DCP unit digitally filters out the unwanted bands and feeds the required data to the external processor.

3.8 System Flow Chart

The system flow chart illustrated below in figure 3.7 explains how the system should deal with different operation mode conditions.

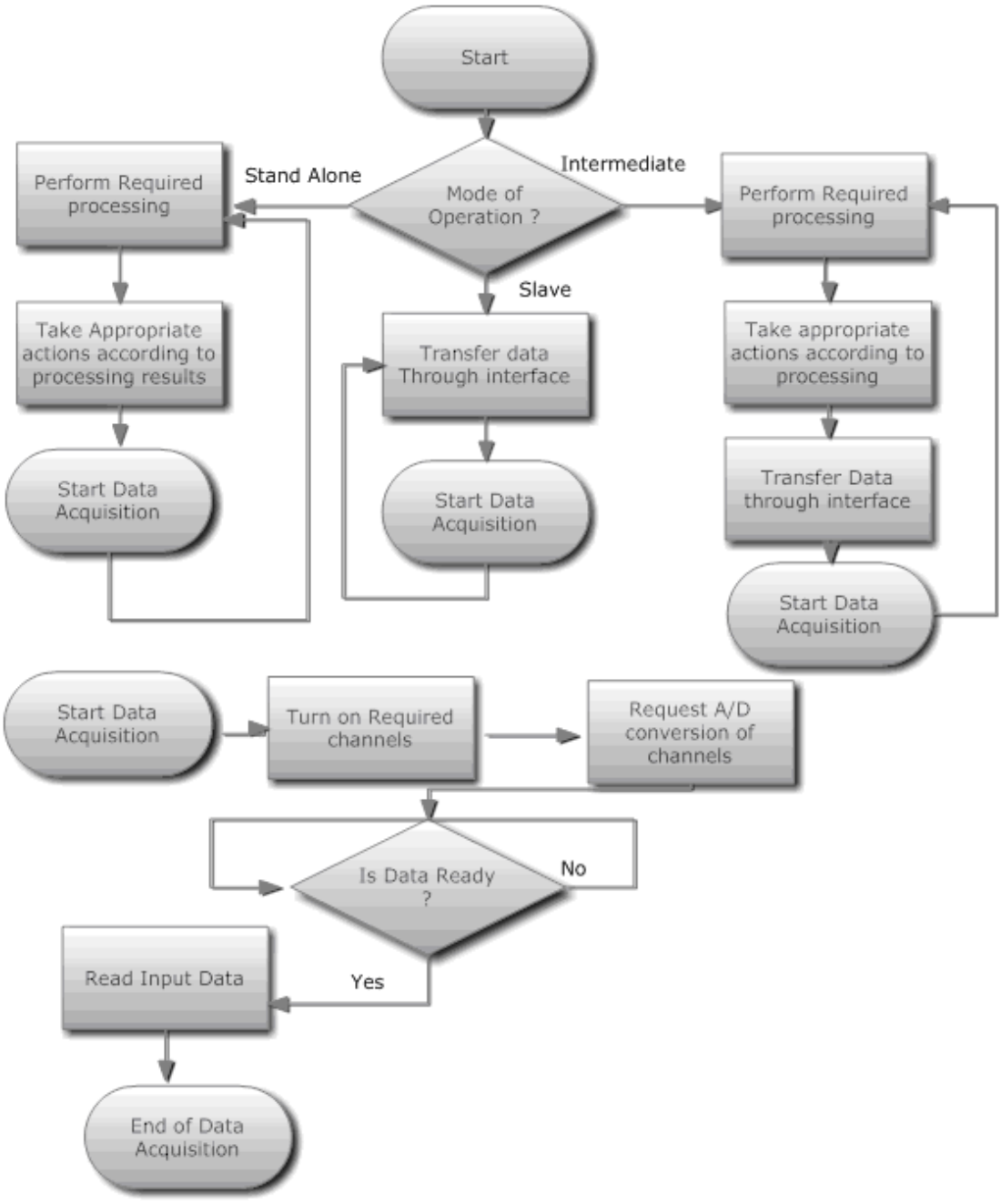


Figure 3.7. **System flow chart.**

3.9 Our Design's Standings

In this section we will conclude this chapter by a comparison between our proposed EEG data acquisition system and the state-of-the-Art systems mentioned in the previous chapter (see Table 3.1).

Table 3.1

State of the Art Comparison

Design	[1]	[3]	[12]	[16]	[17]	[28]	Our Design
Supported Electrodes	Not Mentioned	wet & dry Electrodes	subdural strip electrodes	Dry passive Electrodes and golden/Ag-AgCl	Non-contact capacitive electrodes	cup type electrodes (wet electrodes)	wet & dry Electrodes
# of channels	16	7	-	8	N/A	1	16
Channels Expandability	-	Yes	-	No	Yes	No	Yes
Amp. current Consumption	-	135µA	-	-	1µA	-	135µA
Amplifier Gain	1M	1K	-	6K for dry electrodes 50K for wet electrodes	1.1K	-	1K
Amplifier CMRR	-	135dB	-	-	-	>110dB	135dB
Amplifier Input Noise Voltage	-	14nV/√Hz	-	2 µVpp at 10Hz	-	-	14nV/√Hz
Filter Pass band	0.5-35Hz	1-100 Hz	0. -100	0-100Hz (tunable)	1-100Hz	NM	1-100Hz
ADC resolution (bits)	-	18	12	12 or 16	16	12	24
ADC sampling rate(SPS)	128	2K	200	256	-	47K	1.8 -23.7K
ADC current consumption	-	20 µA	-	-	-	-	8.4mA
Battery operation capability	Yes	Yes	No	Yes	Yes	Yes	Yes
Real time Operation	No	No	-	No	No	No	Yes
Mobility	Yes	Yes	No	Yes	Yes	Yes	Yes

Chapter 4

Prototype Design

4.0 Overview

In this chapter we will discuss in details the physical and design aspects of our proposed system, schematics and printed circuit board design of the system.

4.1 Printed Circuit Board Layout and Design

Printed circuit boards (PCB) is a much safer and noise resistant solution than breadboard circuits used for prototyping purposes, and due to the very sensitive nature of the biosignal we are attempting to process, any testing conducted on noisy layouts has no value. Therefore the goal of this design is to be implemented directly on a PCB to provide better testing conditions and eliminate any other factors from the equation.

Completed schematics and PCB layouts will be discussed in this chapter, also additional implemented PCB layout techniques will be illustrated and we will show how these techniques directly affect the intended performance of the system.

In the next section we will be describing physical dimensions and suggested layout of the proposed system.

4.2 Design Layout

The intended layout of the system is illustrated in figure 4.1; the system is composed of three modules:

1) Analog Front End module (AFE).

2) Digital Control and Processing Module (DCP).

3) Analog to Digital Conversion module (ADC).

Simply the analog front end circuit is a modular based design, each module has 4 channels of input, the AFE modules can be mounted on any of the four sides of the ADC module which provides 360 degree coverage for effective electrodes placement and reduces the electrode wiring effort.

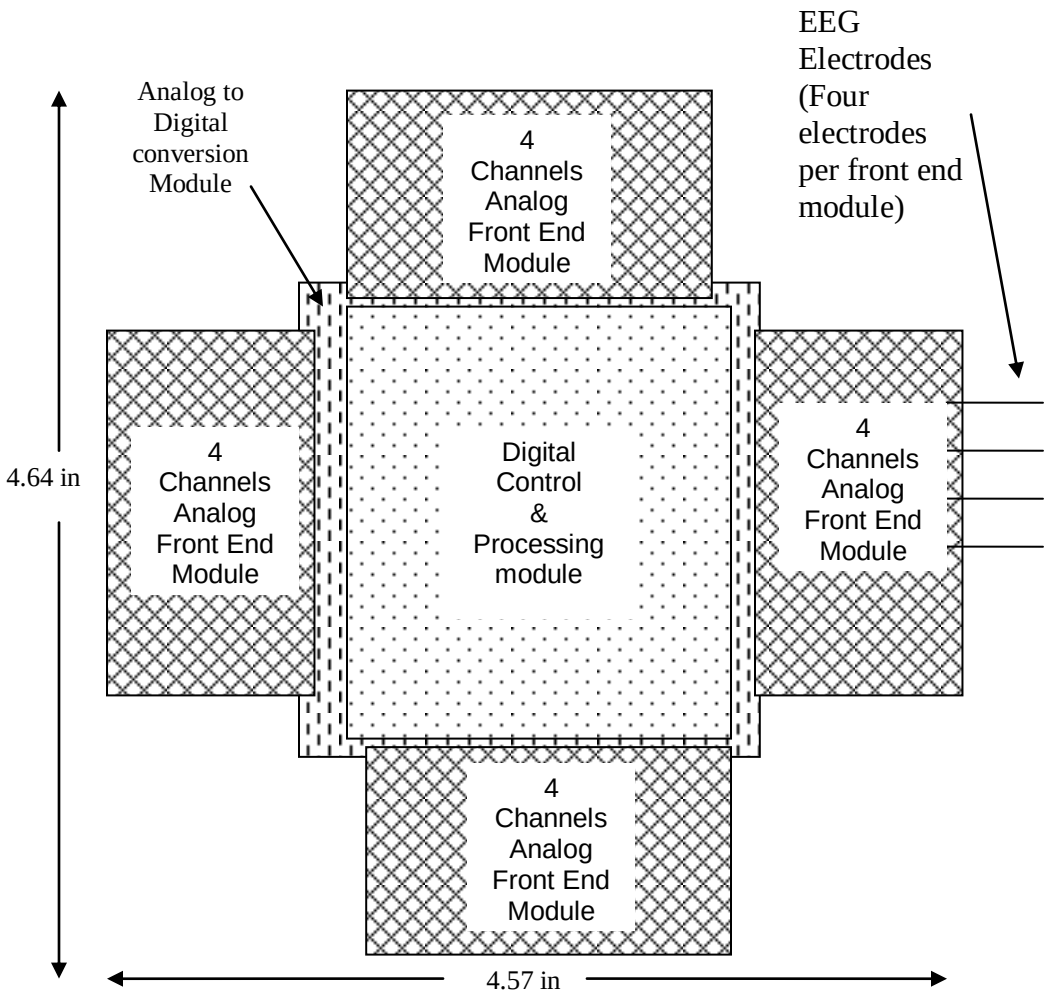


Figure 4.1. **Top view of the system layout.**

The DCP module is housed on top the ADC module, the dimensions of the system is shown in figure 4.1 which is drawn to real size, also figure 4.2 shows an image of the designed system for the sake of size comparison.

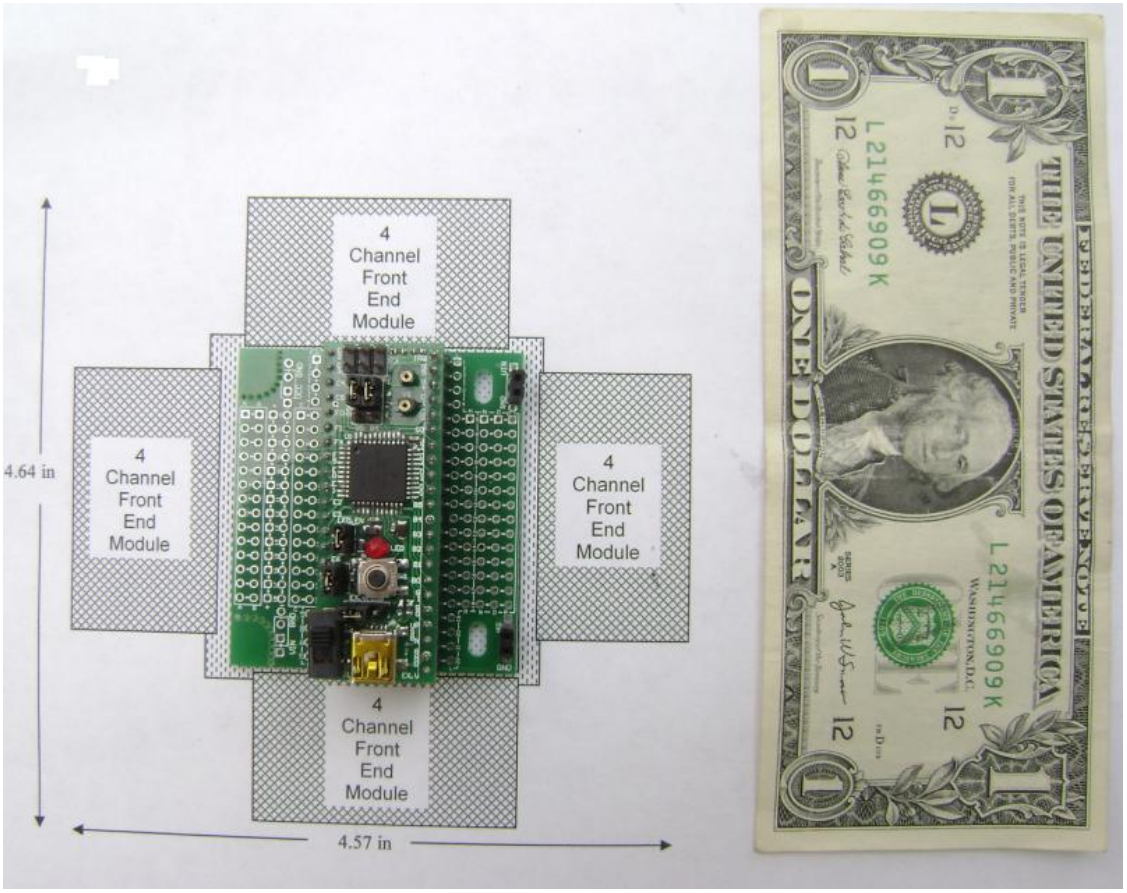


Figure 4.2. **System size comparison.**

In the following sections we will be displaying each designed component's schematic and PCB layout and explaining them in details.

4.3 Analog Front End Module

The complete schematic of a single channel of the front end module is shown in figure 4.3 which shows the differential amplifier circuit, filtering and conditioning circuitry.

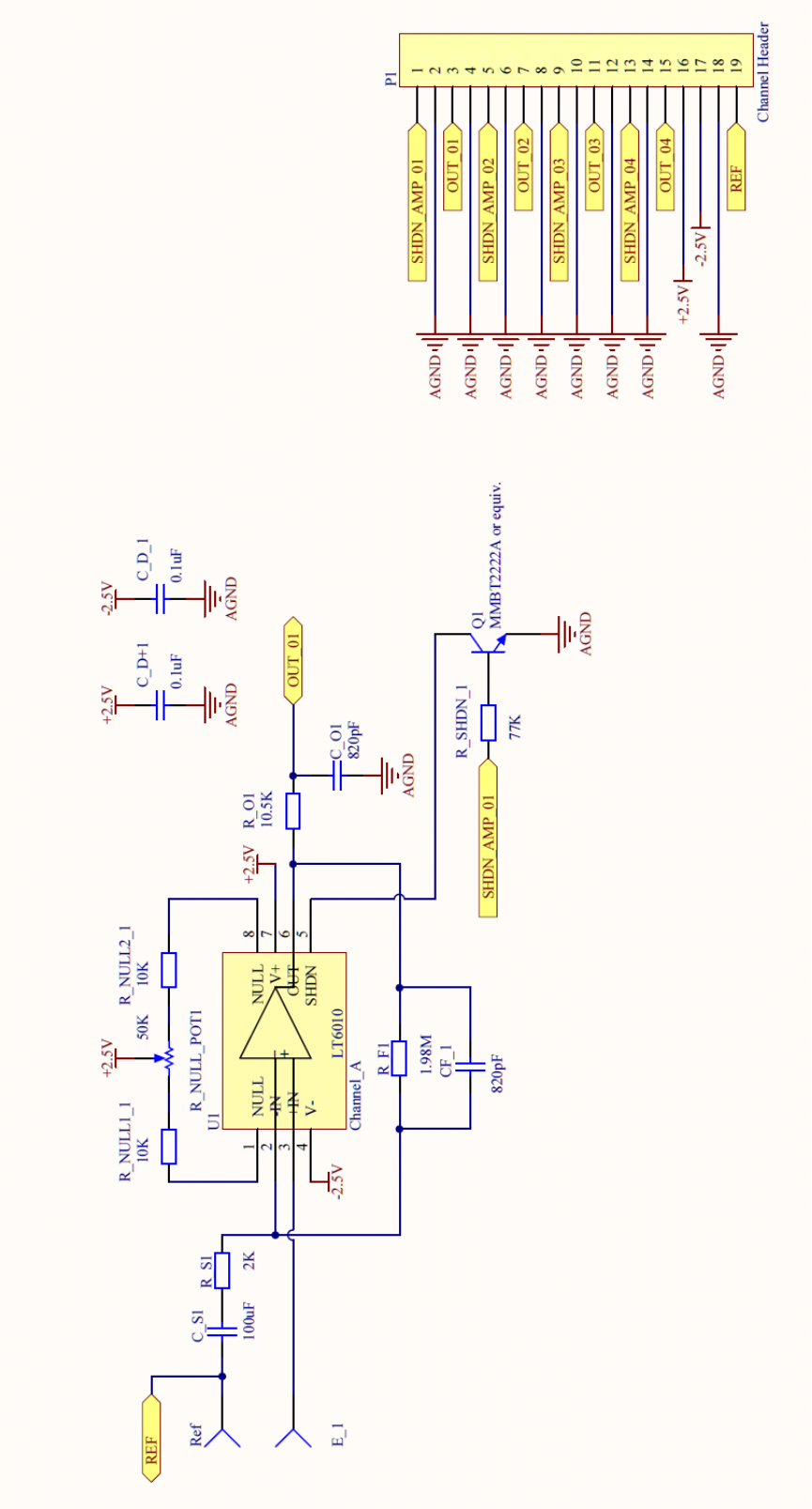


Figure 4.3. **Schematic of the front end circuit.**

A single AFE module consists of four identical channel conditioning circuits, only one channel is shown in figure 4.3 for illustration purposes.

The amplification gain is determined by the ratio of R_F1 to R_S1 which is computed to be approximately 1000. The capacitor C_S1 of value 100 μF acts as a high pass filter only permitting frequencies above 1Hz while C_O1 , C_F1 and R_O1 form two-pole high pass filter with a cutoff frequency of 100 Hz.

The LT6010 can be put into shutdown when the SHDN pin is biased at less than 0.2V above the negative supply (in our case if SHDN <-2.3). The part operates normally when pulled 2V or more above V– (SHDN >-0.5), since the OpAmp is biased using a -2.5 to +2.5 voltage swing to enable bipolar signal amplification. Therefore the common collector circuit (Q1) is placed to bias the SHDN according to the shutdown signal received from the DCP unit.

For the null circuit we placed a 50KΩ potentiometer R_NULL_POT1 to be adjusted for offset voltage cancellation and it is placed between the null pins 1 and 8 of the LT6010 along with two 10KΩ resistors.

The Channel header P1 is a standard 19 pin header connecting the AFE circuit to the ADC module. Every two pins of the P1 header are separated by a ground pin for shielding purposes. The header carries:

- The four channels' outputs.
- The four shutdown inputs.
- Biasing Voltage inputs (+/- 2.5 V).
- Analog ground signal.

Figure 4.4 shows the frequency response of the conditioning channel this was simulated using 5spice software and a standard LT1010 OpAmp since the LT6010's simulation model was not found , the mid band gain is shown to be around 60dB (or 100) in the region between 1 and 100Hz.

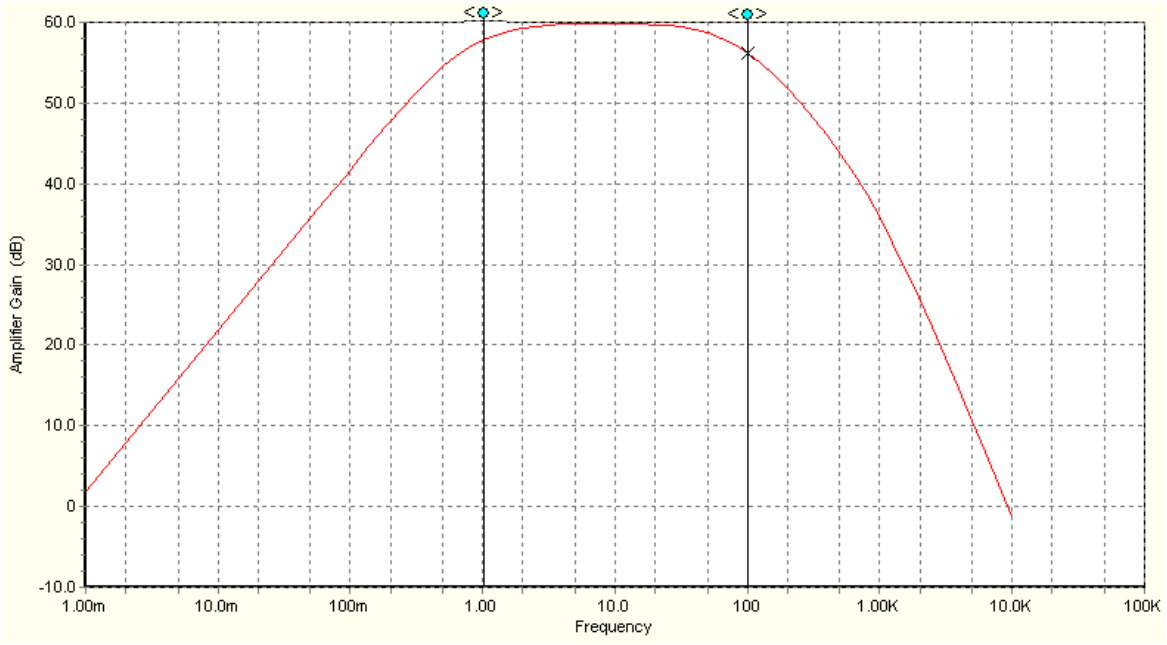


Figure 4.4. **Frequency response of the conditioning channel.**

Figure 4.5a displays a sample input SIN wave of 2µV amplitude and 20Hz frequency and the corresponding output is shown in figure 4.5b. The output is also a SIN wave of amplitude of approximately 2mV, which the input amplified by 1000 gain as designed.

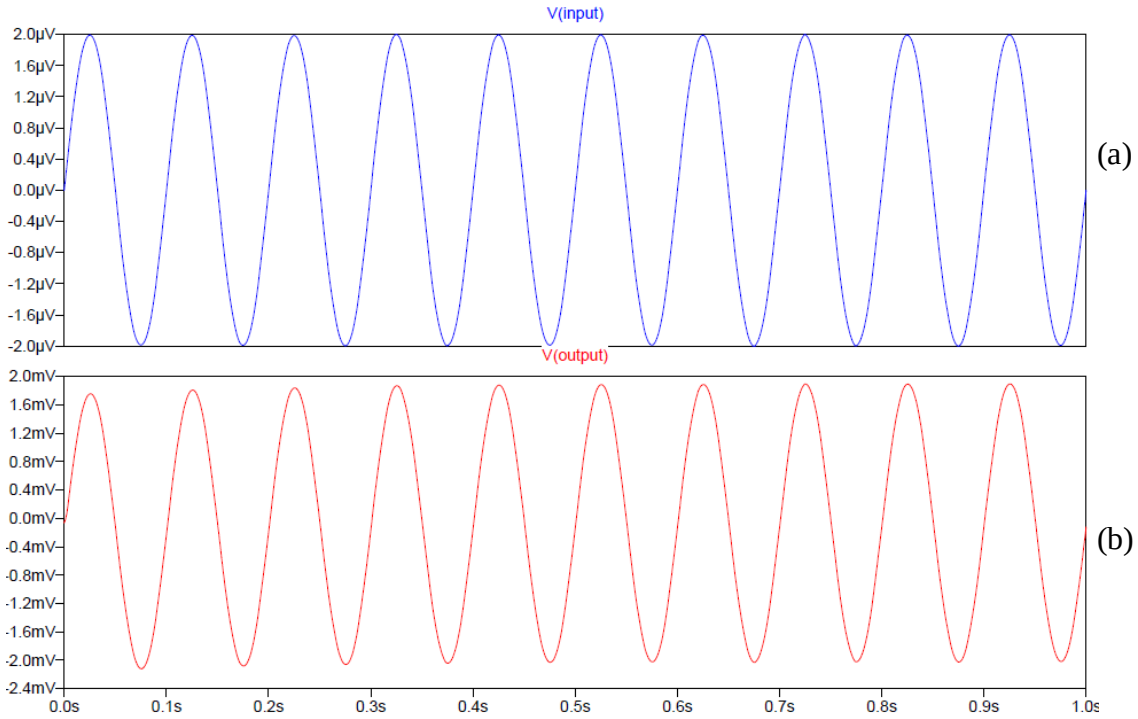


Figure 4.5. **Sample input signal and its output.**

To demonstrate the rail-to-rail functionality of the front end circuit figure 4.6 illustrates the output of a 3mv sin wave input. Notice that the input signal was amplified by the 60dB gain but the the signal above the +2.5V and below -2.5V was cut off due to the OpAmp bias voltage.

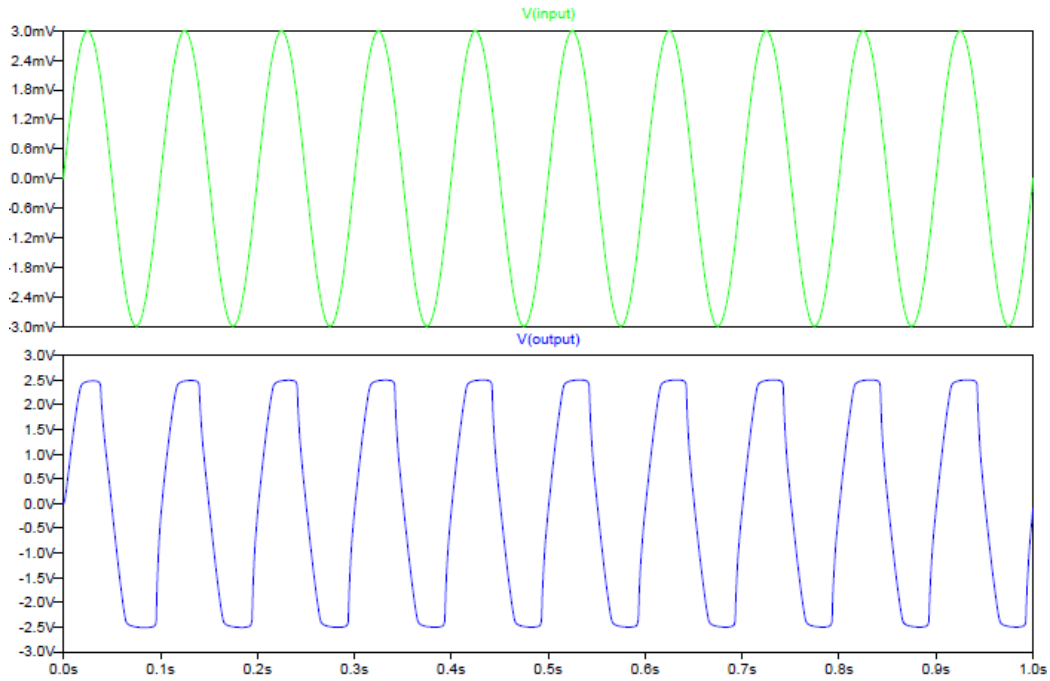


Figure 4.6. **Rail-To-Rail output demo.**

Figure 4.7 shows a simulation of the common mode noise cancellation process. A 1mV noise signal of frequency 60 Hz was applied to both the input 2mV 10Hz signal (Vinput) and to the reference signal (Vreference) to simulate the common noise. The Output is an amplified signal of the difference between the noisy input signal (Vinput+noise) and the reference (Vrefence). Thus the common noise has been canceled and the resulting output is a clean 2 V sin wave of 10Hz frequency with no effect of the 60 Hz common noise.

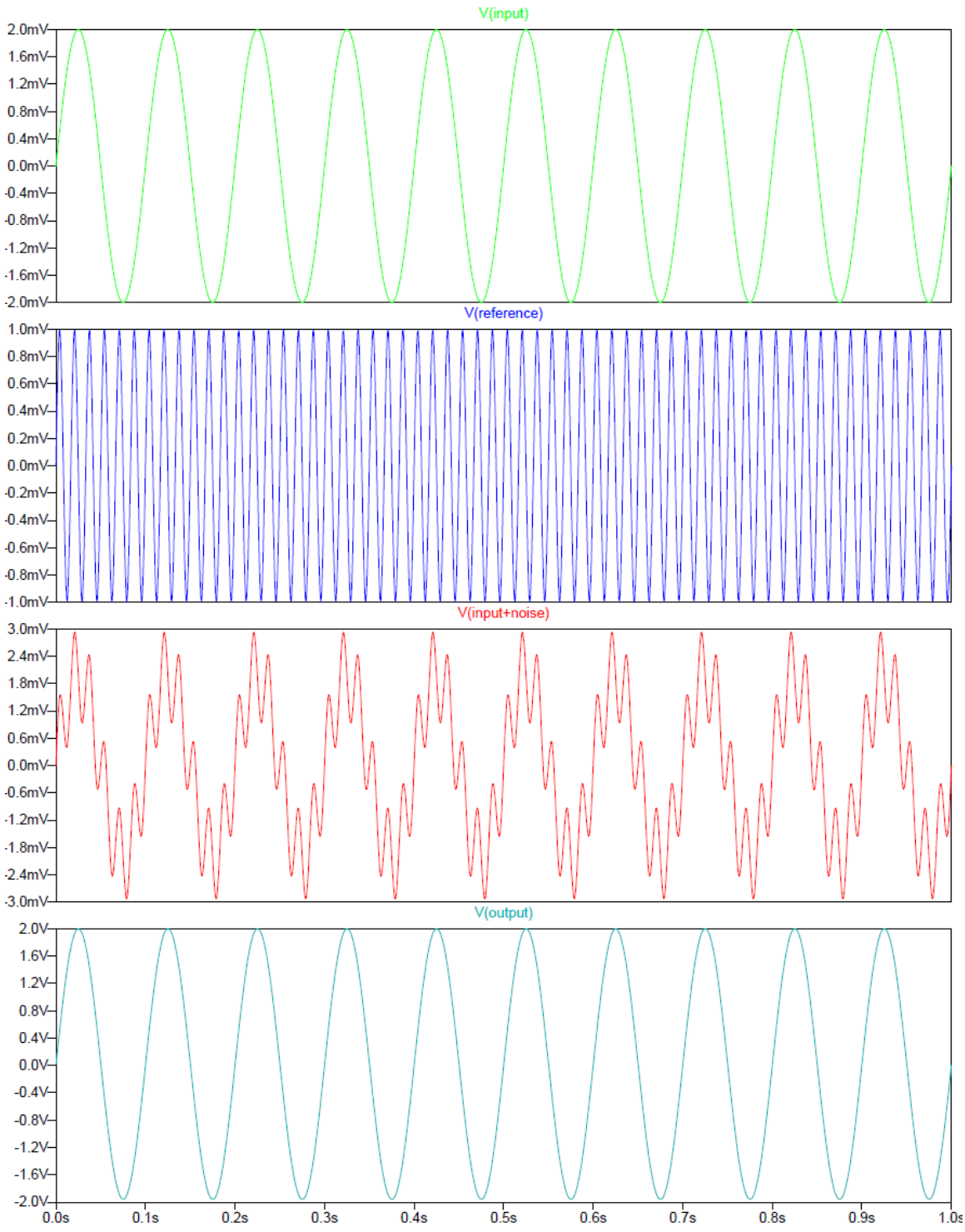


Figure 4.7. **Common noise cancellation**

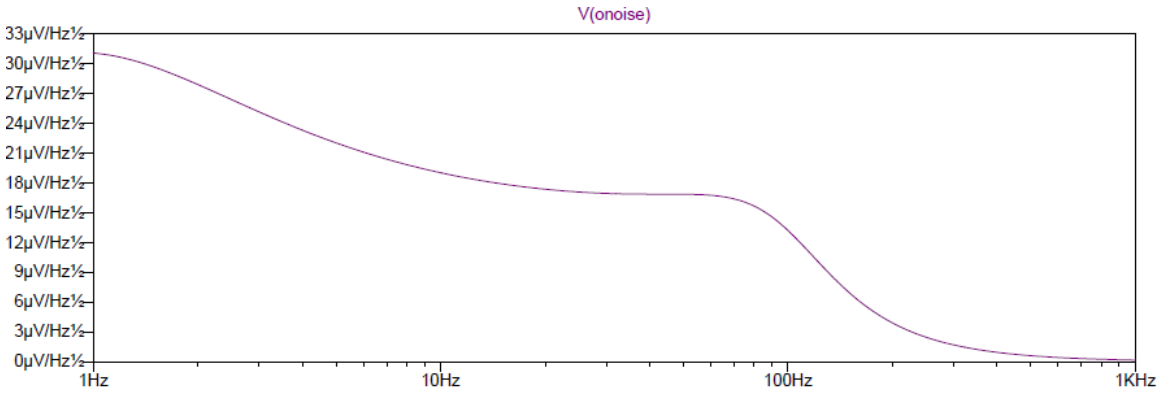


Figure 4.8. **Output noise versus frequency**

Figure 4.8 shows the relation between the output noise versus the frequency .In the 1-100Hz EEG frequency range the output noise starts at approximately 30µV/√Hz and decrease until it reaches 12µV/√Hz at 100 Hz. This outlines the robustness of the system against noise since these micro volt range noise signals would have a minor effect on the millivolt range output of the AFE module.

The designed printed circuit board for the AFE module is shown in figure 4.9. The four front-end channels are illustrated and they are all identical. Channel 4 shown in figure 4.9(a) is detachable in order for it to be placed as a single conditioning channel in the ADC module as will be explained later. Figure 4.9(b) shows the connection header connecting the module to the ADC module.

In figure 4.10, a detailed view is shown of a single conditioning channel, Figure 4.10(a) shows the input electrode connectors' layout surrounded by a guard ring which acts as a shield from interference and this guard ring is also applied at the inputs and outputs of the operational amplifier as shown in figure 4.10(b). Figure 4.10(c) outlines the location of the operational amplifier on the board. The shutdown circuitry controlled

by the transistor Q1 is shown in Figure 4.10(d). Figure 4.10(e) points to the detachment holes for the channel to be separated from the module.

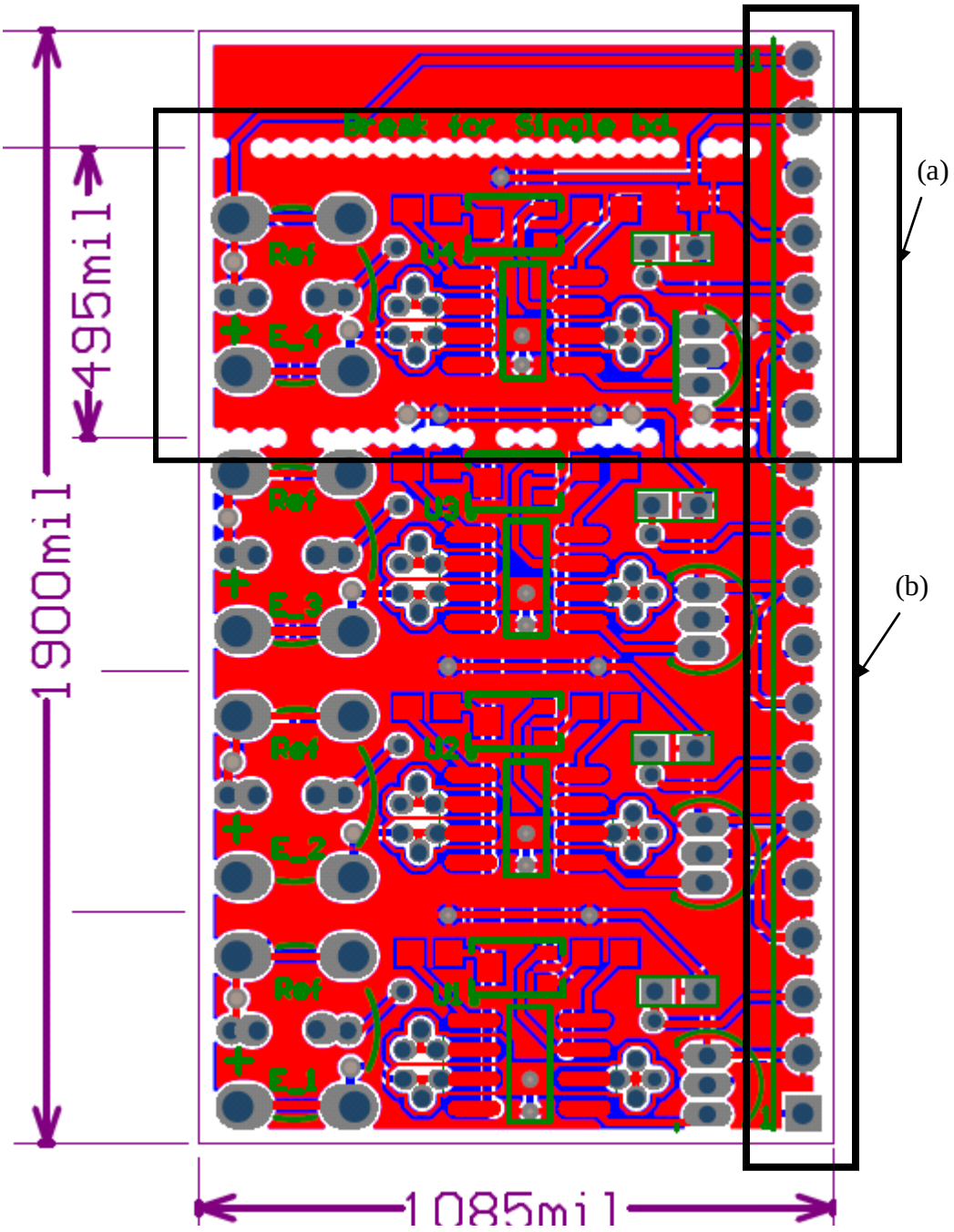


Figure 4.9. **The PCB layout of the front end module.**

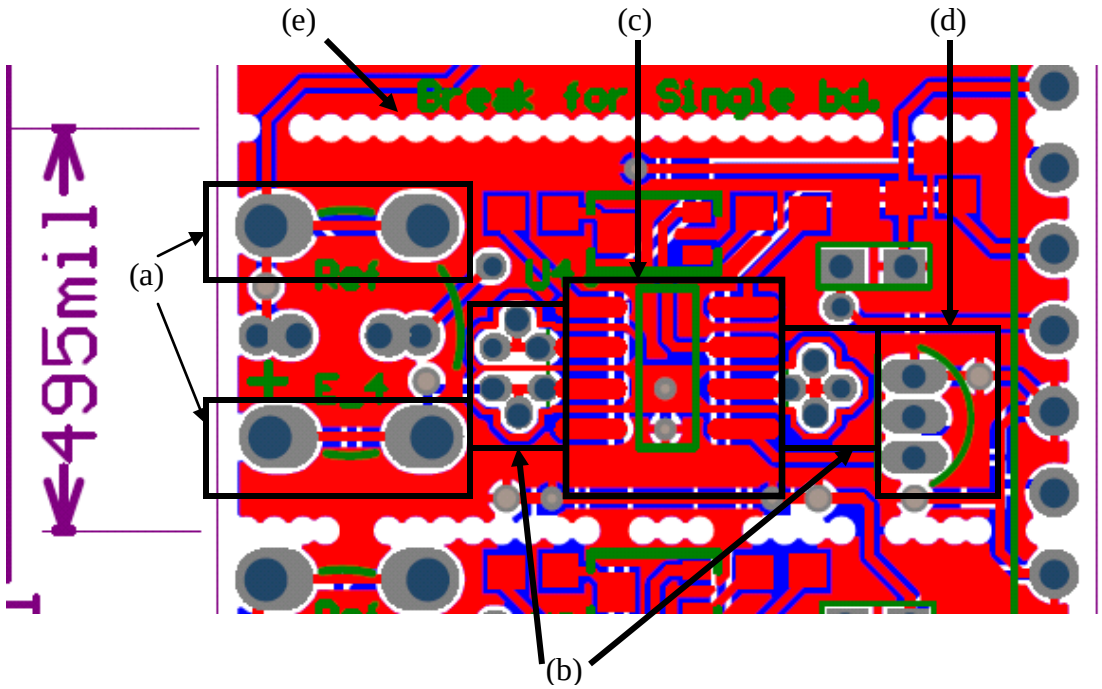


Figure 4.10. **PCB layout for a single channel.**

Table 4.1 lists the bill of materials used in the AFE module.

Table 4.1

Bill of Materials of the AFE Module

Description	Designator	Quantity	Specification
Capacitor	CF_1-4	4	820 pF
Capacitor	C_D+1-4 , C_D_1-4	8	0.1 μF
Capacitor	C_O1-04	4	820 pF
Capacitor	C_S1-4	4	100 μF
Electrode Socket	E_1-4	4	Standard 2mm male/female
Ref Socket	Ref 1-4	4	Standard 2mm male/female
Channel HDR	Header 19 pins P1	1	Standard 19 pin header
Transistor	Q1-4	4	MMBT2222A or equiv.
Resistor	R_F1-4	4	1.98 MΩ
Resistor	R_NULL1_1-4, R_NULL2_1-4	8	10 KΩ
Resistor	R_SHDN_1-4	4	77 KΩ
Potentiometer	R_NULL_POT1-4	4	50 KΩ
Resistor	R_O1-4	4	10.5 KΩ
Resistor	R_S1-4	4	2 KΩ
Operational Amplifier	U1-4	4	LT6010

4.4 Analog to Digital Conversion Module

The ADC module design is composed of four schematics. The first schematic (ADC SCH01) shown in figure 4.11 has the connectors of the ADC module to the other system components. Headers P1, P2, P3 and P4 are the interface to the AFE modules to

gather all the 16 channels data. Connectors J1 and J2 are connected to the ground probe and the reference probe respectively.

The header P5 is the connector between the ADC module and the DCP unit. It carries the following signals:

- The 8 GPIO pins.
- The SPI data connection pins: Master Out Slave In (MOSI), Master In Slave Out (MISO) and the SPI clock (SPSCLK1).
- The ADC chip control pins to the DCP unit such as the data ready (A-D DRDY) , start ADC conversion (A-D start), ADC reset (A-D RESET),the ADC chip select (A-D CS), and the ADC power down (A-D PWDN).
- The shutdown control signal for the optional additional conditioning stage (SHDN_2nd_AMP).
- The digital ground signal (DVDD).
- The negative voltage supply (-5v).

We have completely isolated the digital ground from the analog ground in our design in order to eliminate interference and they only meet at header P6 where they are connected together. Header P7 is where the additional conditioning circuitry could be placed between the multiplexer's output and the ADC's input.

The second schematic shown in figure 4.12 contains the main components of the ADC module, the ADS1258 is connected to the analog inputs (Out_01 to Out_16), the 8 GPIO bits and the data and control signals from the DCP unit connected through header P5 in (ADC SCH01).

The reference circuit in (ADC SCH02) was designed per the instructions of the manufacturer of the ADC chip [26]. It provides a clean reference voltage to the ADC for conversion. Header P9 is a jumper that provides the option to select the sampling clock source by connecting the CLKSEL pin to ground the ADC's clock is used generated by the 32.7 KHz crystal.

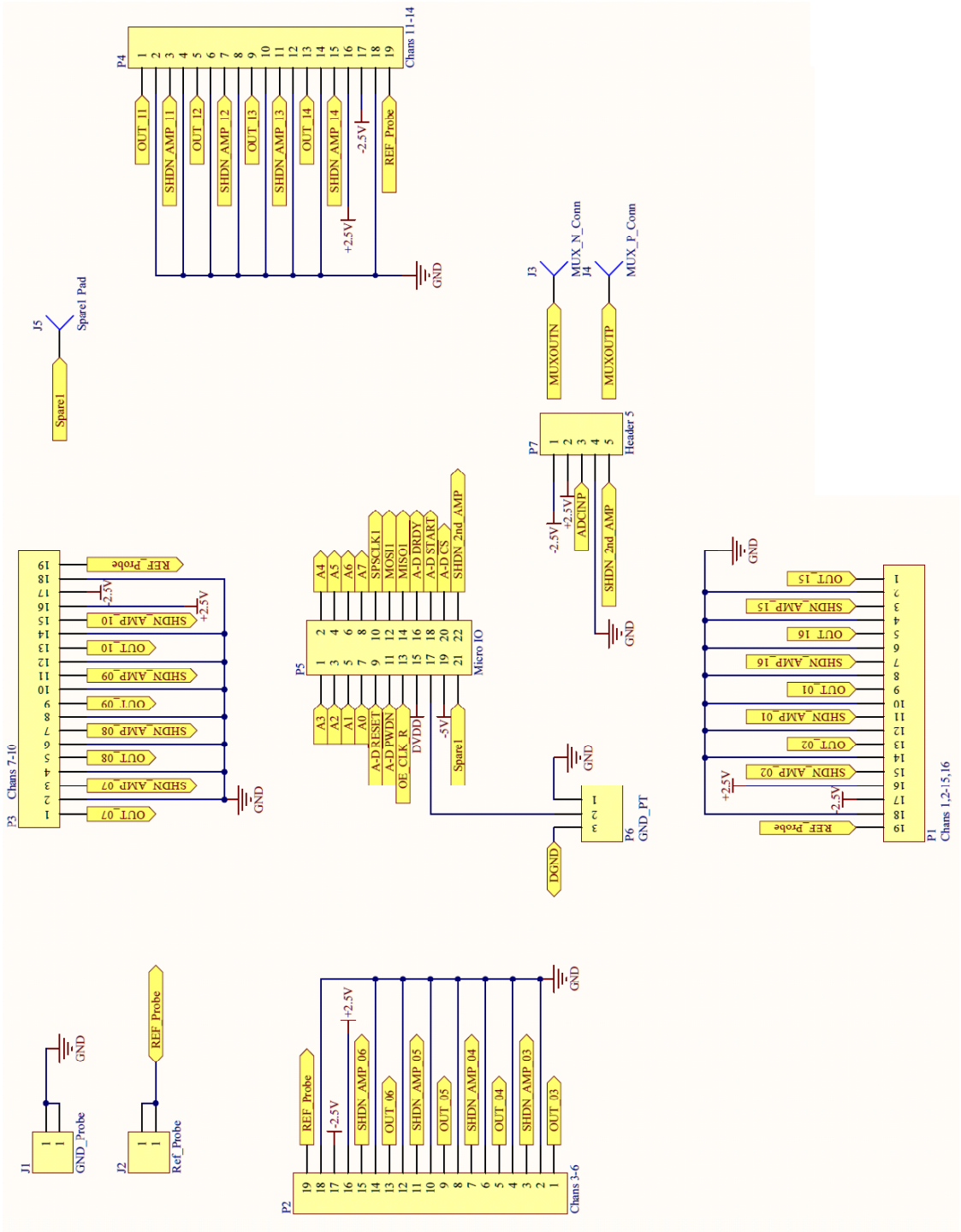


Figure 4.11. **ADC interface schematic (ADC SCH01).**

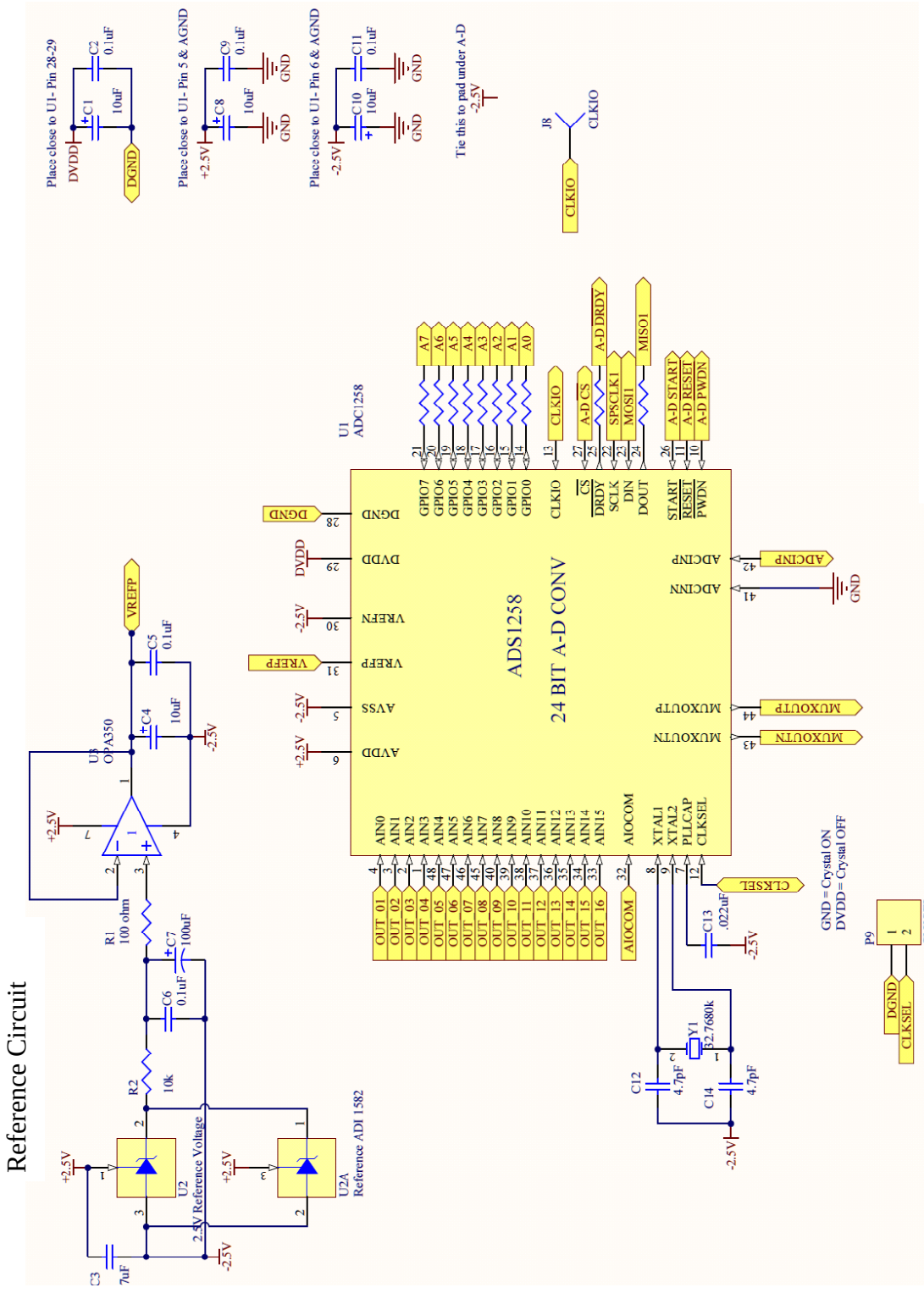


Figure 4.12. **ADC main schematic (ADC SCH02).**

The third schematic of the ADC module (ADC SCH03) shown in figure 4.13 illustrates the shutdown control design. The two shift registers (MC54HC595AJ) are 8-bit serial-input/serial or parallel-output shift register, they receive the data serially through the SPI port from the DCP unit and translate it into parallel signals addressing the shut down circuits of each analog channel.

Also (ADC SCH03) shows the two power conditioning circuits that convert the +5 and -5 supply voltages into +2.5 and -2.5 voltages respectively. The header P8 is a jumper that allows the choice to connect the reference electrode to either the analog ground or the ADC common input.

The Last schematic of the ADC module design (ADC SCH04) in figure 4.14 contains the protection circuits where two zenner diodes are placed at each analog input to the ADC to ensure the input is within the -2.5 to +2.5V voltage range in order to prevent any voltage increase hazards to the ADC.

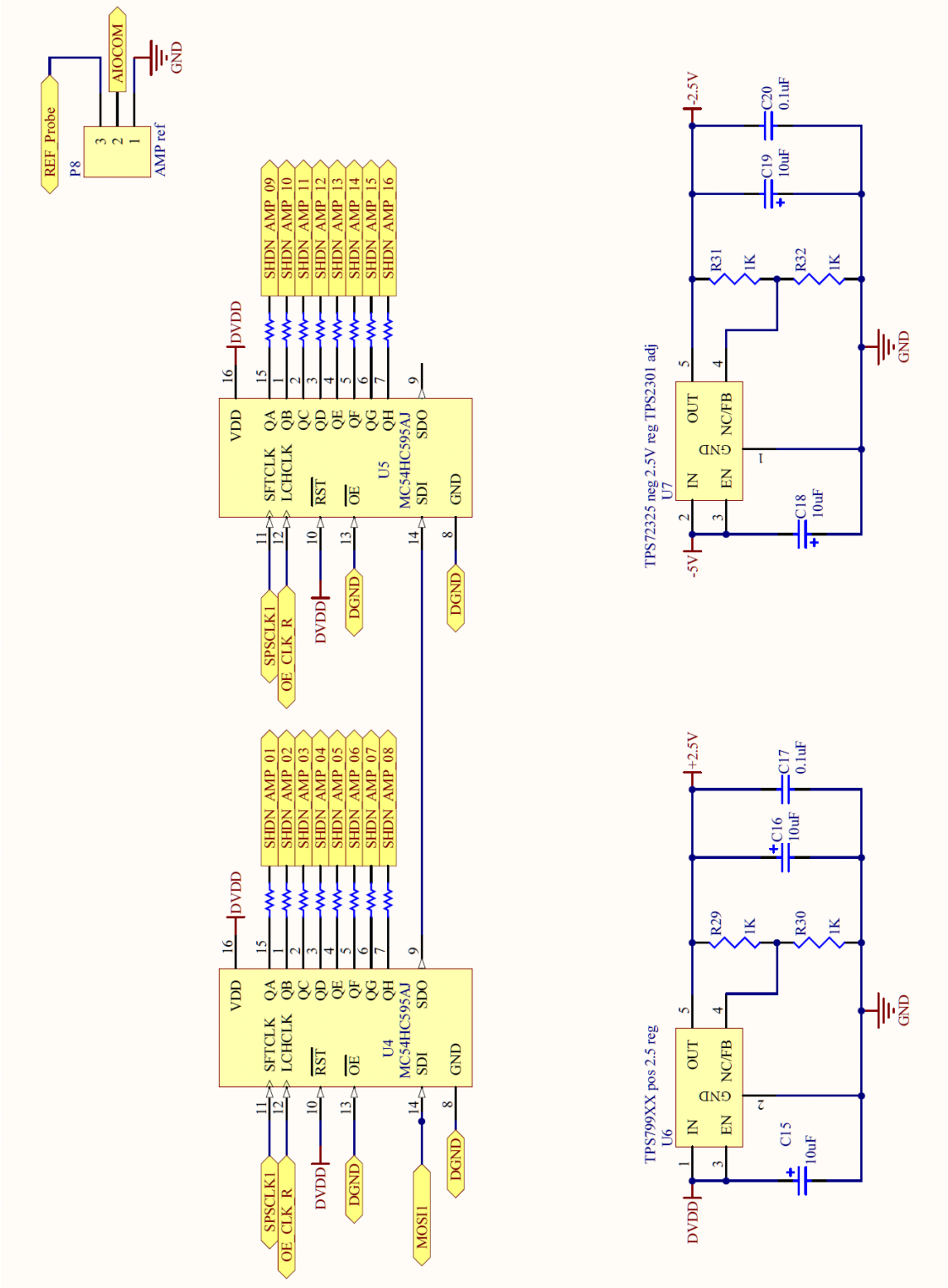


Figure 4.13. **Shutdown control schematic (ADC SCH03).**

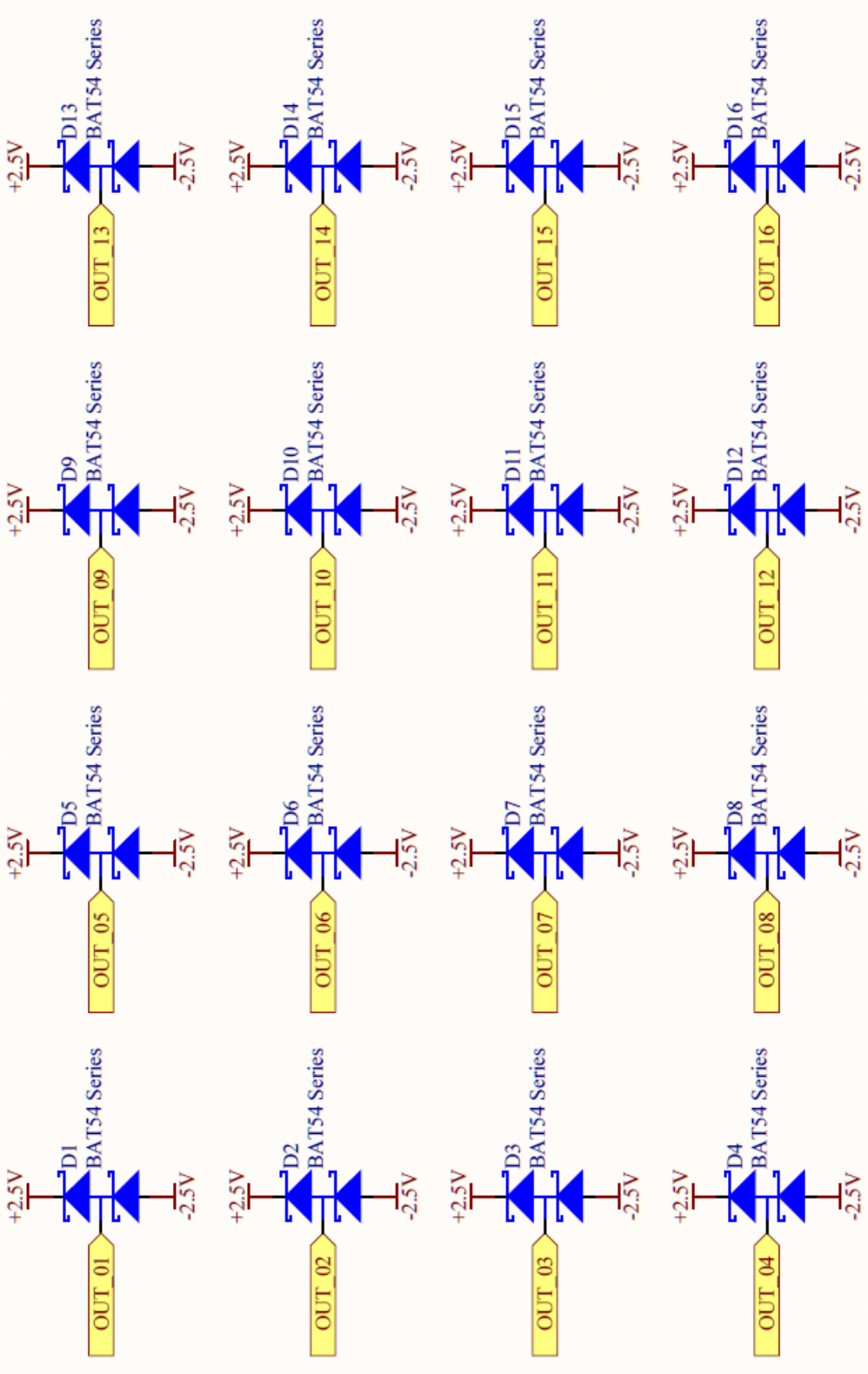


Figure 4.14. **Zenner diode input protection (ADC SCH04).**

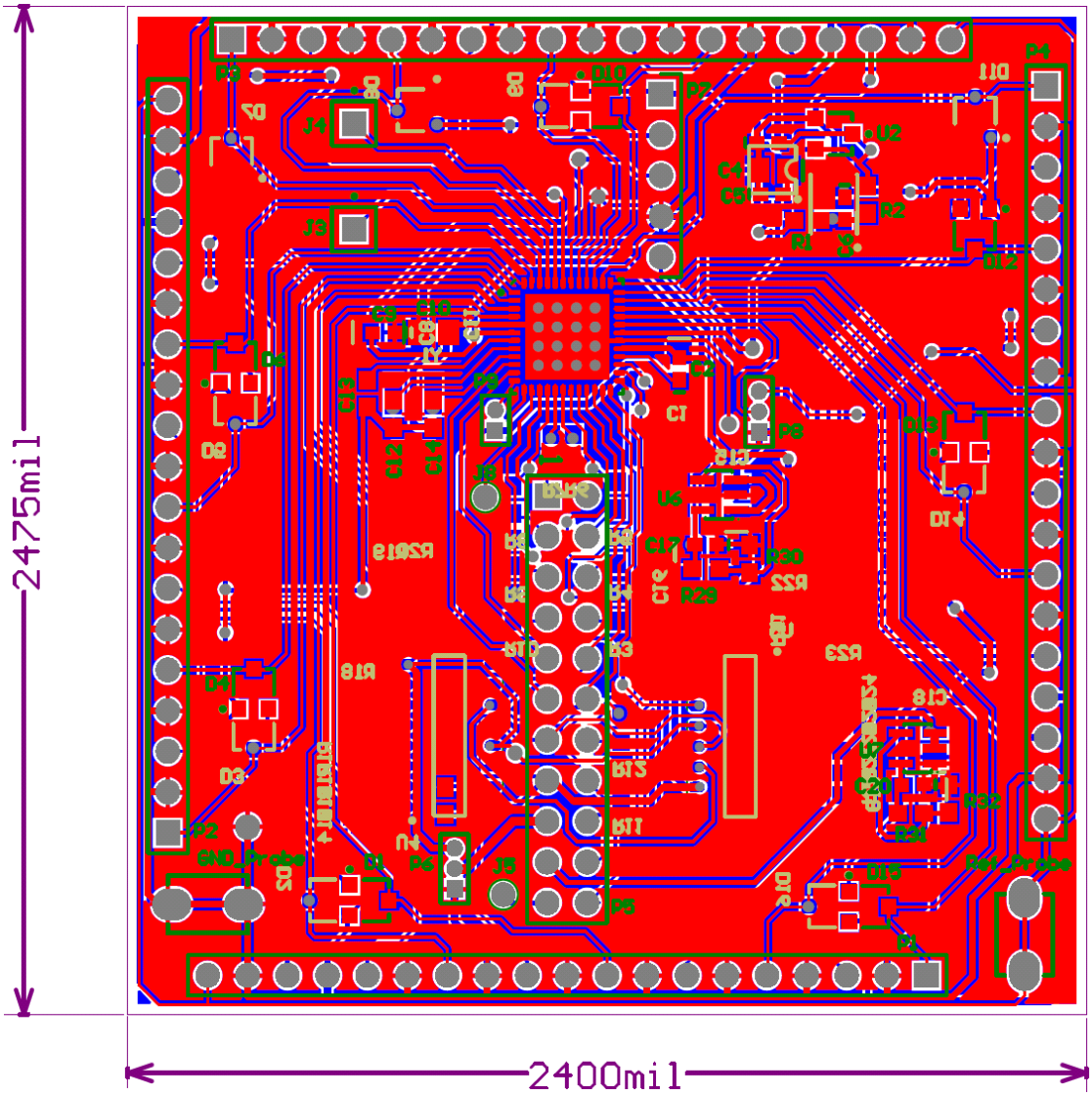


Figure 4.15. **ADC module PCB layout.**

Figure 4.15 shows the PCB of the ADC module, it is a double layer 5.94 squared inch board.

4.5 Digital Control and Processing Module

For the DCP unit we have used the JM development board which is a product of the Computer Group. It is based on the MCF51JM128 microcontroller and is accompanied by a prototyping board for additional components to be added to the development board. Figure 4.16 shows an image of the JM development and the prototyping board.

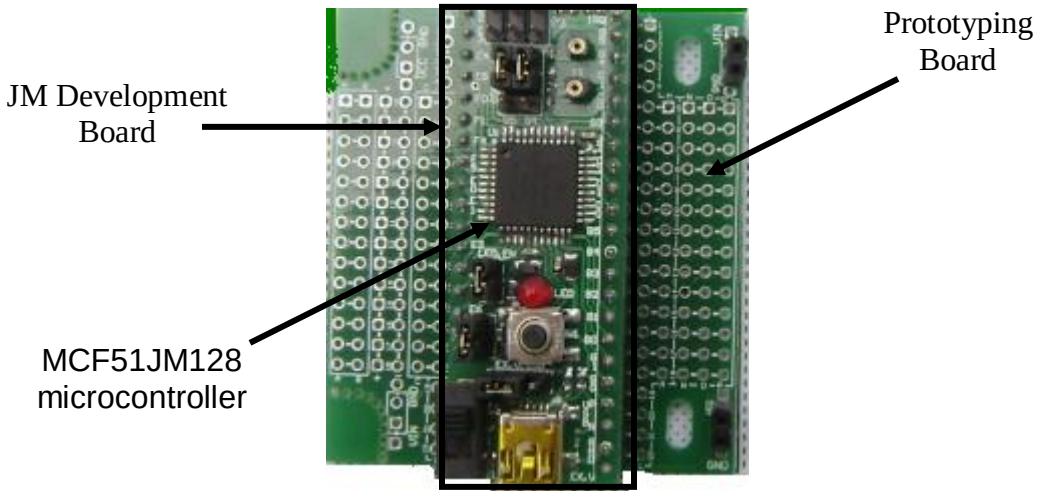


Figure 4.16. **DCP module actual images.**

The DCP unit is connected using a 22 pins header attached to the prototyping board and connecting it to the ADC module. This header is connected to the header P5 in schematic (ADC SCH01) mentioned earlier. The schematics and PCB designs for the DCP module are provided courtesy of the Computer Group and are shown in figures 4.17 and 4.18 respectively.

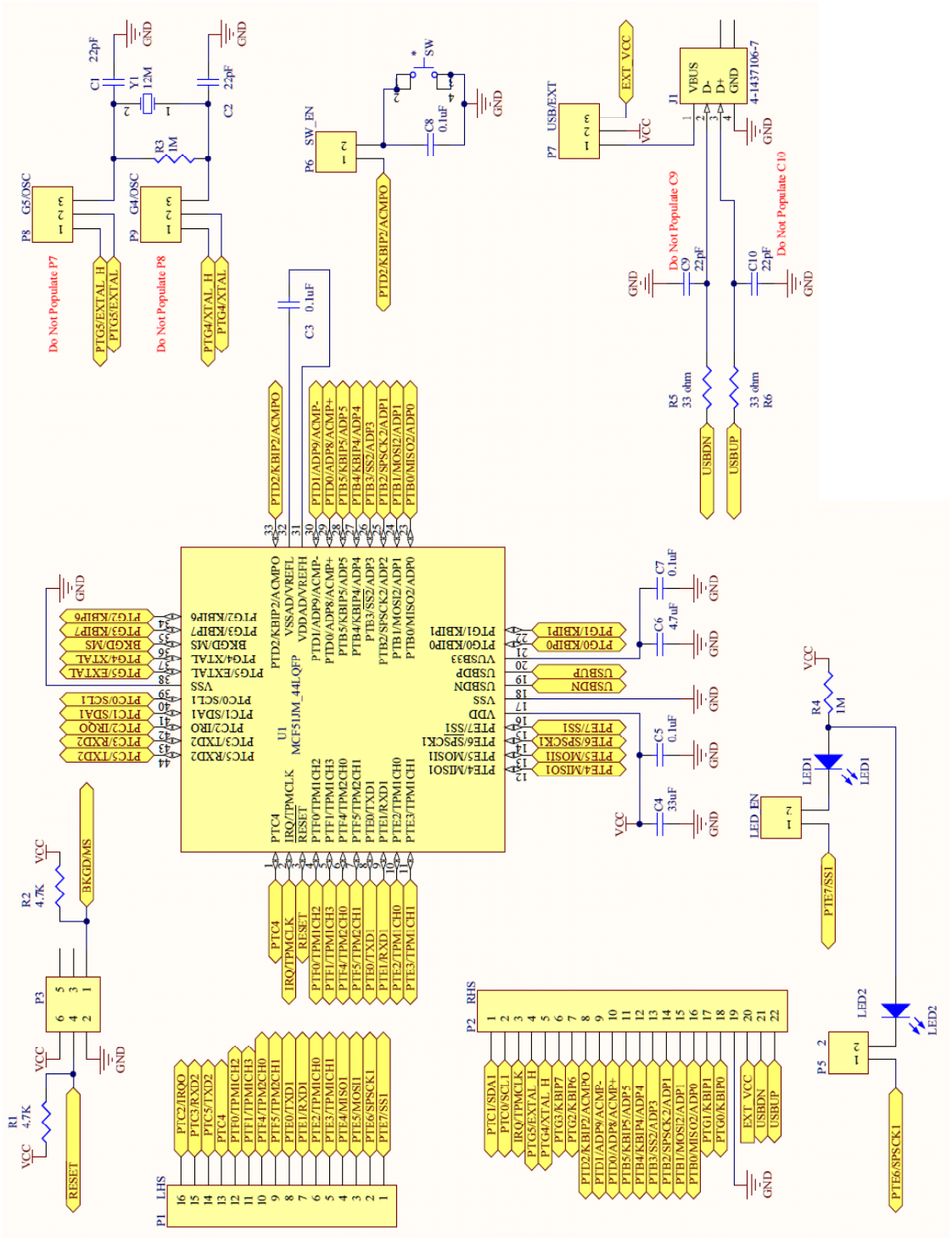


Figure 4.17. **DCP module schematic.**

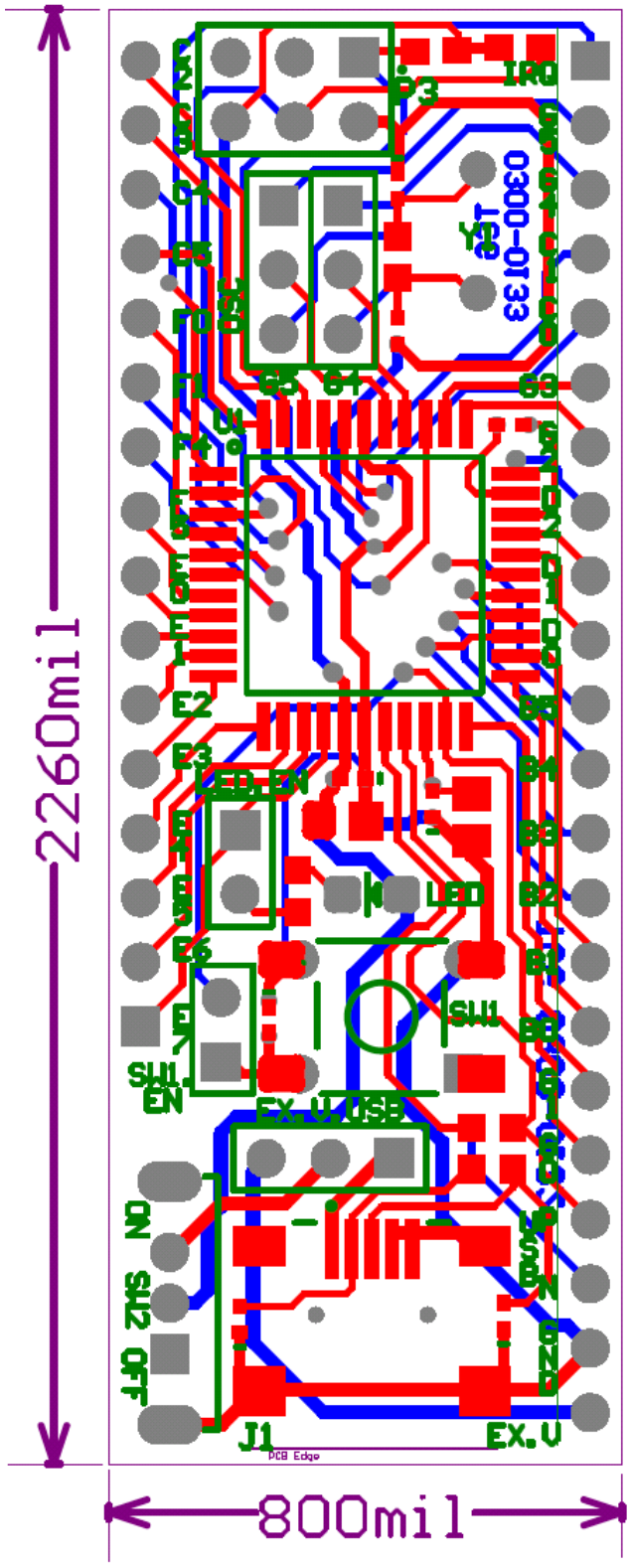


Figure 4.18. **DCP module PCB layout.**

Chapter 5

Conclusion and Future Research

5.0 Summary

As we have shown EEG based applications are being introduced massively in our day to day life and most likely would have a great impact on our future. It is being used in various medical applications and its role is vital in the diagnosis of certain diseases such as epilepsy [27] . It is also projected to be used in the consumer market in products such as gaming, automotive and communication products.

BCI design faces many limitations such as noise, low power, mobility and electrode compatibility. State of the art BCI systems also lack the intelligent control interface that allows complete management of the data acquisition system that is separated from the processing end.

We have taken on the responsibility of designing an intelligent data acquisition system which addresses the discussed issues and is a flexible development platform for researcher to carry on their investigations providing them with reliable data and suppleness to customize their products in order to serve their needs.

Our system is composed of three independent modules that could be interconnected. The first module is the analog front module (AFE) which is responsible for the analog signal acquisition, amplification and filtering. The AFE modules' outputs are transferred to the second module which is the analog to digital conversion (ADC)

module. The ADC module converts the analog input into digital data that is ready to be stored or analyzed. And this whole process is managed using a flexible and customizable digital control module (DCP) that is microcontroller based.

Our system complies with the state of the art specifications, it supports low power operation for mobile applications, and it is also very robust against noise and external interference which is a major concern in BCI design. Our system is compatible with both dry and wet electrodes supporting both conventional applications and novel mobile applications.

We have provided schematics and printed circuit board designs for the complete system, proposed the theory of operation and a comparison was carried out between our design and the state of the art products.

5.1 Future Research

Our design is a solution to the data acquisition limitations of the EEG based applications however a room of improvements is still available. Due to the ease of adding components to digital component of the design, wireless operation could be added to the system by simply attaching a Zigbee transceiver to the system which would be a great addition for monitoring and remote control applications.

Also, since our three modules designs are completely independent any module could be replaced by a more advanced one but taking into consideration the pin compatibility of the modules. For example the analog front end could be replaced by another design depending on the researcher's needs and that wouldn't affect the behavior of the other system components.

If more signal processing tasks are required by the DCP module, the used MCF51JM128 microcontroller could be replaced by another processor which is capable of signal processing activities.

Finally the design should be implemented and tested on human subjects to fine tune the noise and conditioning levels.

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